STC12C5A60S2 series MCU
STC12LE5A60S2 series MCU
Data Sheet

STC MCU Limited
www.STCMCU.com

Update date: 2011-1-13
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Chapter 1. Introduction

STC12C5A60S2 is a single-chip microcontroller based on a high performance 1T architecture 80C51 CPU, which is produced by STC MCU Limited. With the enhanced kernel, STC12C5A60S2 executes instructions in 1~6 clock cycles (about 6~7 times the rate of a standard 8051 device), and has a fully compatible instruction set with industrial-standard 80C51 series microcontroller. In-System-Programming (ISP) and In-Application-Programming (IAP) support the users to upgrade the program and data in system. ISP allows the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in Flash memory while the application program is running. The STC12C5A60S2 retains all features of the standard 80C51. In addition, the STC12C5A60S2 has two extra I/O ports (P4 and P5), a 10-sources, 4-priority-level interrupt structure, 10-bit ADC, two UARTs, on-chip crystal oscillator, a 2-channel PCA and PWM, SPI, a one-time enabled Watchdog Timer.

1.1 Features

- Enhanced 80C51 Central Processing Unit ,1T per machine cycle, faster 6~7 times than the rate of a standard 8051.
- Operating voltage range: 5.5V ~ 3.5V or 2.2V ~ 3.6V (STC12LE5A60S2).
- Operating frequency range: 0- 35MHz, is equivalent to standard 8051:0~420MHz.
- On-chip 8/16/20/40/48/52/56/60/62K FLASH program memory with flexible ISP/IAP capability.
- On-chip 1280 byte RAM.
- Be capable of addressing up to 64K byte of external RAM.
- Dual Data Pointer (DPTR) to speed up data movement.
- Power control: idle mode(all interrupt can wake up IDLE mode) and power-down mode(external interrupt can wake up Power-Down mode).
- Code protection for flash memory access.
- Excellent noise immunity, very low power consumption.
- Four 16-bit timer/counter, be compatible with Timer0/Timer1 of standard 8051, 2-channel PCA can be available as two timers.
- 10 vector-address, 4 level priority interrupt capability.
- One enhanced UART with hardware address-recognition and frame-error detection function.
- Secondary UART with self baud-rate generator.
- One 15 bits Watch-Dog-Timer with 8-bit pre-scaler (one-time-enabled).
- SPI Master/Slave communication interface.
- Two channel Programmable Counter Array (PCA).
- 10-bit, 8-channel Analog-to-Digital Converter (ADC).
- Simple internal RC oscillator and external crystal clock.
- Three power management modes: idle mode, slow down mode and power-down mode.
- Power down mode can be woken-up by PCA_pin, RXD_pin, T0/T1 pin and external interrupts (INT0, INT1).
- Maximum 44 programmable I/O ports are available.
- Programmable clock output Function. T0 output the clock on P3.4, T1 output the clock on P3.5, BRT output the clock on P1.0.
- External low-voltage detector function(P4.6, the EA pin at the pin location of standard 8051).
1.2 Block diagram

The CPU kernel of STC12C5A60S2 is fully compatible to the standard 8051 microcontroller, maintains all instruction mnemonics and binary compatibility. With some great architecture enhancements, STC12C5A60S2 executes the fastest instructions per clock cycle. Improvement of individual programs depends on the actual instructions used.
1.3 Pin Configurations

LQFP-48
STC12C5A60S2

PDIP-40
STC12C5A60S2
## 1.4 Pin Descriptions

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>LQFP44</th>
<th>LQFP48</th>
<th>PDIP40</th>
<th>PLCC44</th>
<th>QFN40</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0.0 ~ P0.7</td>
<td>37-30</td>
<td>40 ~ 33</td>
<td>39-32</td>
<td>43 ~ 36</td>
<td>34 ~ 27</td>
<td>Port0: Port0 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory.</td>
</tr>
<tr>
<td>P1.0/ADC0/CLKOUT2</td>
<td>40</td>
<td>43</td>
<td>1</td>
<td>2</td>
<td>36</td>
<td>Port1: General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port1, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high.</td>
</tr>
<tr>
<td>P1.1/ADC1</td>
<td>41</td>
<td>44</td>
<td>2</td>
<td>3</td>
<td>37</td>
<td>ADCn: Analog to Digital Converter Input</td>
</tr>
<tr>
<td>P1.2/ADC2/EC1/RxD2</td>
<td>42</td>
<td>45</td>
<td>3</td>
<td>4</td>
<td>38</td>
<td>Port2: Port2 is an 8-bit bi-directional I/O port with pull-up resistance. Except being as GPIO, Port2 emits the high-order address byte during accessing to external program and data memory.</td>
</tr>
<tr>
<td>P1.3/ADC3/CCP0/TxD2</td>
<td>43</td>
<td>46</td>
<td>4</td>
<td>5</td>
<td>39</td>
<td>Port3: General-purposed I/O with weak pull-up resistance inside. When 1s are written into Port3, the strong output driving CMOS only turn-on two period and then the weak pull-up resistance keep the port high. Port3 also serves the functions of various special features of STC12C5A60S2.</td>
</tr>
<tr>
<td>P1.4/ADC4/CCP1/SS</td>
<td>44</td>
<td>47</td>
<td>5</td>
<td>6</td>
<td>40</td>
<td>Port4: Port4 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P1.5/ADC5/MOSI</td>
<td>1</td>
<td>2</td>
<td>6</td>
<td>7</td>
<td>1</td>
<td>Port5: Port5 are extended I/O ports such like Port1. It can be available only on LQFP48.</td>
</tr>
<tr>
<td>P1.6/ADC6/MISO</td>
<td>2</td>
<td>3</td>
<td>7</td>
<td>8</td>
<td>2</td>
<td>Port6: Port6 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P1.7/ADC7/SCLK</td>
<td>3</td>
<td>4</td>
<td>8</td>
<td>9</td>
<td>3</td>
<td>Port7: Port7 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P2.0 ~ P2.7</td>
<td>18 - 25</td>
<td>19 - 23</td>
<td>21 - 28</td>
<td>24 - 31</td>
<td>16 - 23</td>
<td>Port8: Port8 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.0/RXD</td>
<td>5</td>
<td>6</td>
<td>10</td>
<td>11</td>
<td>5</td>
<td>Port9: Port9 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.1/TXD</td>
<td>7</td>
<td>8</td>
<td>11</td>
<td>13</td>
<td>6</td>
<td>Port10: Port10 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.2/INT0</td>
<td>8</td>
<td>9</td>
<td>12</td>
<td>14</td>
<td>7</td>
<td>Port11: Port11 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.3/INT1</td>
<td>9</td>
<td>10</td>
<td>13</td>
<td>15</td>
<td>8</td>
<td>Port12: Port12 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.4/T0/INT/CLKOUT0</td>
<td>10</td>
<td>11</td>
<td>14</td>
<td>16</td>
<td>9</td>
<td>Port13: Port13 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.5/T1/INT/CLKOUT1</td>
<td>11</td>
<td>12</td>
<td>15</td>
<td>17</td>
<td>10</td>
<td>Port14: Port14 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.6/WR</td>
<td>12</td>
<td>13</td>
<td>16</td>
<td>18</td>
<td>11</td>
<td>Port15: Port15 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P3.7/RD</td>
<td>13</td>
<td>14</td>
<td>17</td>
<td>19</td>
<td>12</td>
<td>Port16: Port16 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.0/SS</td>
<td>17</td>
<td>18</td>
<td>23</td>
<td></td>
<td></td>
<td>Port17: Port17 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.1/ECI/MOSI</td>
<td>28</td>
<td>31</td>
<td>34</td>
<td></td>
<td></td>
<td>Port18: Port18 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.2/CCP0/MISO</td>
<td>39</td>
<td>42</td>
<td>1</td>
<td></td>
<td></td>
<td>Port19: Port19 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.3/CCP1/SCLK</td>
<td>6</td>
<td>7</td>
<td>12</td>
<td></td>
<td></td>
<td>Port20: Port20 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.4/NA</td>
<td>26</td>
<td>29</td>
<td>29</td>
<td>32</td>
<td>24</td>
<td>Port21: Port21 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.5/ALE</td>
<td>27</td>
<td>30</td>
<td>30</td>
<td>33</td>
<td>25</td>
<td>Port22: Port22 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.6/EX_LVD/RST2</td>
<td>29</td>
<td>32</td>
<td>31</td>
<td>35</td>
<td>26</td>
<td>Port23: Port23 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P4.7/RST</td>
<td>4</td>
<td>5</td>
<td>9</td>
<td>10</td>
<td>4</td>
<td>Port24: Port24 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>RST</td>
<td>4</td>
<td>5</td>
<td>9</td>
<td>10</td>
<td>4</td>
<td>Port25: Port25 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P5.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port26: Port26 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P5.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port27: Port27 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P5.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port28: Port28 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>P5.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port29: Port29 are extended I/O ports such like Port1. It can be available only on LQFP44, LQFP48, PLCC44.</td>
</tr>
<tr>
<td>XTAL1</td>
<td>15</td>
<td>16</td>
<td>19</td>
<td>21</td>
<td>14</td>
<td>Crystal1: Input to the inverting oscillator amplifier. Receives the external oscillator signal when an external oscillator is used.</td>
</tr>
<tr>
<td>XTAL2</td>
<td>14</td>
<td>15</td>
<td>18</td>
<td>20</td>
<td>13</td>
<td>Crystal2: Output from the inverting amplifier. This pin should be floated when an external oscillator is used.</td>
</tr>
<tr>
<td>VCC</td>
<td>38</td>
<td>41</td>
<td>40</td>
<td>44</td>
<td>35</td>
<td>Power</td>
</tr>
<tr>
<td>Gnd</td>
<td>16</td>
<td>17</td>
<td>20</td>
<td>22</td>
<td>15</td>
<td>Ground</td>
</tr>
</tbody>
</table>
1.5 Pin Drawings

LQFP-44 OUTLINE PACKAGE

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-</td>
<td>-</td>
<td>1.60</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>-</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
</tr>
<tr>
<td>c1</td>
<td>0.09</td>
<td>-</td>
<td>0.16</td>
</tr>
<tr>
<td>D</td>
<td>12.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>10.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>12.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>10.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>b (w/o plating)</td>
<td>0.25</td>
<td>0.30</td>
<td>0.35</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.60</td>
<td>0.75</td>
</tr>
<tr>
<td>L1</td>
<td>1.00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>θ</td>
<td>0°</td>
<td>3.5°</td>
<td>7°</td>
</tr>
</tbody>
</table>

NOTES:
1. JEDEC OUTLINE: MS-026 BSB
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
LQFP-48 OUTLINE PACKAGE

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-</td>
<td>-</td>
<td>1.60</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>-</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>1.40</td>
<td>1.45</td>
</tr>
<tr>
<td>A3</td>
<td>0.59</td>
<td>0.64</td>
<td>0.69</td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>-</td>
<td>0.27</td>
</tr>
<tr>
<td>b1</td>
<td>0.17</td>
<td>0.20</td>
<td>0.23</td>
</tr>
<tr>
<td>c</td>
<td>0.13</td>
<td>-</td>
<td>0.18</td>
</tr>
<tr>
<td>c1</td>
<td>0.12</td>
<td>0.127</td>
<td>0.134</td>
</tr>
<tr>
<td>D</td>
<td>8.80</td>
<td>9.00</td>
<td>9.20</td>
</tr>
<tr>
<td>D1</td>
<td>6.90</td>
<td>7.00</td>
<td>7.10</td>
</tr>
<tr>
<td>E</td>
<td>8.80</td>
<td>9.00</td>
<td>9.20</td>
</tr>
<tr>
<td>E1</td>
<td>6.90</td>
<td>7.00</td>
<td>7.10</td>
</tr>
<tr>
<td>e</td>
<td>-</td>
<td>-</td>
<td>0.50</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.60</td>
<td>0.75</td>
</tr>
<tr>
<td>L1</td>
<td>1.00REF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>0.08</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>R2</td>
<td>0.08</td>
<td>-</td>
<td>0.20</td>
</tr>
<tr>
<td>S</td>
<td>0.20</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
PDIP-40 OUTLINE PACKAGE

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>MIN</th>
<th>NOR</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-</td>
<td>-</td>
<td>0.190</td>
</tr>
<tr>
<td>A1</td>
<td>0.015</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>A2</td>
<td>0.015</td>
<td>0.155</td>
<td>0.160</td>
</tr>
<tr>
<td>C</td>
<td>0.008</td>
<td>-</td>
<td>0.015</td>
</tr>
<tr>
<td>D</td>
<td>2.025</td>
<td>2.060</td>
<td>2.070</td>
</tr>
<tr>
<td>E</td>
<td>0.600</td>
<td>BSC</td>
<td></td>
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<tr>
<td>E1</td>
<td>0.540</td>
<td>0.545</td>
<td>0.550</td>
</tr>
<tr>
<td>L</td>
<td>0.120</td>
<td>0.130</td>
<td>0.140</td>
</tr>
<tr>
<td>θ</td>
<td>0.630</td>
<td>0.650</td>
<td>0.670</td>
</tr>
<tr>
<td>θ</td>
<td>0</td>
<td>0</td>
<td>15</td>
</tr>
</tbody>
</table>

NOTE:
1. JEDEC OUTLINE : MS-011 AC
PLCC-44 OUTLINE PACKAGE

NOTE:

1. JEDEC OUTLINE: M0-047 AC

2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DIMENSIONS E AND D DO NOT INCLUDE MODE PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION.

<table>
<thead>
<tr>
<th>SYMBOLS</th>
<th>DIMENSIONS IN INCH</th>
<th>DIMENSIONS IN MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.165 - 0.180</td>
<td>4.191 - 4.572</td>
</tr>
<tr>
<td>A1</td>
<td>0.020 - -</td>
<td>0.508 - -</td>
</tr>
<tr>
<td>A2</td>
<td>0.147 - 0.158</td>
<td>3.734 - 4.013</td>
</tr>
<tr>
<td>b1</td>
<td>0.026 0.028 0.032</td>
<td>0.660 0.711 0.813</td>
</tr>
<tr>
<td>b</td>
<td>0.013 0.017 0.021</td>
<td>0.330 0.432 0.533</td>
</tr>
<tr>
<td>c</td>
<td>0.007 0.010 0.0013</td>
<td>0.178 0.254 0.330</td>
</tr>
<tr>
<td>D</td>
<td>0.650 0.653 0.656</td>
<td>16.510 16.586 16.662</td>
</tr>
<tr>
<td>E</td>
<td>0.650 0.653 0.656</td>
<td>16.510 16.586 16.662</td>
</tr>
<tr>
<td>e</td>
<td>0.050BSC</td>
<td>1.270BSC</td>
</tr>
<tr>
<td>Gd</td>
<td>0.590 0.610 0.630</td>
<td>14.986 15.494 16.002</td>
</tr>
<tr>
<td>Ge</td>
<td>0.590 0.610 0.630</td>
<td>14.986 15.494 16.002</td>
</tr>
<tr>
<td>Hd</td>
<td>0.685 0.690 0.695</td>
<td>17.399 17.526 17.653</td>
</tr>
<tr>
<td>He</td>
<td>0.685 0.690 0.695</td>
<td>17.399 17.526 17.653</td>
</tr>
<tr>
<td>L</td>
<td>0.100 - 0.112</td>
<td>2.540 - 2.845</td>
</tr>
<tr>
<td>Y</td>
<td>- - 0.004</td>
<td>- - 0.102</td>
</tr>
</tbody>
</table>
QFN-40 OUTLINE PACKAGE
1.6 STC12C5A60S2 series MCU naming rules

STC12  xx  5A  xx  xx  --  37  x  -  xxxx  xx

- Pin Number
  e.g. 40, 44, 48

- Package type
  e.g. PDIP, LQFP, PLCC

- Temperature range
  I: Industrial, -40℃ - 80℃
  C: Commercial, 0℃ - 70℃

- Operating frequency
  37: Up to 37MHz

- S2: Have Secondary UART, ADC function, PWM and internal EEPROM
- AD: Have ADC function, PWM and internal EEPROM, no Secondary UART
- PWM: Have PWM and internal EEPROM, no Secondary UART and ADC function

- Program space
  08: 8KB
  16: 16KB
  20: 20KB
  20: 20KB
  32: 32KB
  40: 40KB
  48: 60KB
  etc.

- RAM is up to 1280 Bytes

- Operating Voltage
  C: 5.5V~3.3V
  LE: 2.2V~3.6V

STC 1T Series 8051 MCU
Speed is 8~12 times the traditional 8051

1.7 Global unique identification number (ID)

STC 1T MCU 12C5Axx series, each MCU has a unique identification number (ID). User can use “MOV @Ri” instruction read RAM unit F1~F7 to get the ID number after power on.
Chapter 2. Clock, Power Management, Reset

2.1 Clock

2.1.1 Clock Network

There are two clock sources available for STC12C5A60S2. One is the clock from crystal oscillation and the other is from internal simple RC oscillator. The internal built-in RC oscillator can be used to replace the external crystal oscillator in the application which doesn't need an exact system clock. To enable the built-in oscillator, user should enable the option Internal Clock by STC Writer/Programmer.

User can slow down the MCU by means of writing a non-zero value to the CLKS[2:0] bits in the CLK_DIV register. This feature is especially useful to save power consumption in idle mode as long as the user changes the CLKS[2:0] to a non-zero value before entering the idle mode.

CLK_DIV register (Clock Divider)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CLKS2</td>
<td>CLKS1</td>
<td>CLKS0</td>
</tr>
</tbody>
</table>

B2-B0 (CLKS2-CLKS0):
- 000 clock source is not divided (default state)
- 001 clock source is divided by 2.
- 010 clock source is divided by 4.
- 011 clock source is divided by 8.
- 100 clock source is divided by 16.
- 101 clock source is divided by 32.
- 110 clock source is divided by 64.
- 111 clock source is divided by 128.
2.1.2 Internal RC Oscillator frequency (Internal clock frequency)

STC 1T MCU 12C5Ax series in addition to traditional external clock, but also the option of using the internal RC oscillator clock source. If select internal RC oscillator, external crystal can be saved. XTAL1 and XTAL2 floating. Relatively large errors due to internal clock, so high requirements on the timing or circumstances have serial communication is not recommended to use the internal oscillator. User can use “MOV @Ri” instruction read RAM unit FC~FF to get the internal oscillator frequency of the factory and read RAM unit F8~FB to get internal oscillator frequency of last used to download programs within the internal oscillator after power on.
2.2 Power Management

**PCON register** (Power Control Register)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
<td>IDL</td>
</tr>
</tbody>
</table>

- **SMOD**: Double baud rate of UART interface
  - 0: Keep normal baud rate when the UART is used in mode 1, 2, or 3.
  - 1: Double baud rate bit when the UART is used in mode 1, 2, or 3.

- **SMOD0**: SM0/FE bit select for SCON.7; setting this bit will set SCON.7 as Frame Error function. Clearing it to set SCON.7 as one bit of UART mode selection bits.

- **LVDF**: Pin Low-Voltage Flag. Once low voltage condition is detected (VCC power is lower than LVD voltage), it is set by hardware (and should be cleared by software).

- **POF**: Power-On flag. It is set by power-off-on action and can only cleared by software.

- **GF1**: General-purposed flag 1

- **GF0**: General-purposed flag 0

- **PD**: Power-Down bit.

- **IDL**: Idle mode bit.

In initialization program, judge whether POF/PCON.4 have been set or not.

- POF=1, Yes: cold boot Power-On Reset
- POF=0, No: external manual reset or WDT reset or software reset or others

Clear POF/PCON.4
2.2.1 Idle Mode

An instruction that sets IDL/PCON.0 causes that to be the last instruction executed before going into the idle mode, the internal clock is gated off to the CPU but not to the interrupt, timer, PCA, SPI, ADC, WDT and serial port functions. The PCA can be programmed either to pause or continue operating during Idle. The CPU status is preserved in its entirety: the RAM, Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. Timer 0, Timer 1, PWM timer and UART will continue to function during Idle mode.

There are two ways to terminate the idle. Activation of any enabled interrupt will cause IDL/PCON.0 to be cleared by hardware, terminating the idle mode. The interrupt will be serviced, and following RETI, the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits (GFO and GF1) can be used to give an indication if an interrupt occurred during normal operation or during Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way to wake-up from idle is to pull RESET high to generate internal hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

2.2.2 Slow Down Mode

A divider is designed to slow down the clock source prior to route to all logic circuit. The operating frequency of internal logic circuit can therefore be slowed down dynamically, and then save the power.

User can slow down the MCU by means of writing a non-zero value to the CLKS[2:0] bits in the CLK_DIV register. This feature is especially useful to save power consumption in idle mode as long as the user changes the CLKS[2:0] to a non-zero value before entering the idle mode.

**CLK_DIV register (Clock Divider)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CLKS2</td>
<td>CLKS1</td>
<td>CLKS0</td>
</tr>
</tbody>
</table>

B2-B0 (CLKS2-CLKS0):  
000  clock source is not divided (default state)  
001  clock source is divided by 2.  
010  clock source is divided by 4.  
011  clock source is divided by 8.  
100  clock source is divided by 16.  
101  clock source is divided by 32.  
110  clock source is divided by 64.  
111  clock source is divided by 128.
Clock Structure

SYSclk

CLKS2, CLKS1, CLKS0

Not-divided
÷2
÷4
÷8
÷16
÷32
÷64
÷128

Internal system clock (To CPU and peripherals)
2.2.3 Power Down (PD) Mode

An instruction that sets PD/PCON.1 cause that to be the last instruction executed before going into the Power-Down mode. In the Power-Down mode, the on-chip oscillator and the Flash memory are stopped in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-Down. The contents of on-chip RAM and SFRs are maintained. The power-down mode can be woken-up by RESET pin, external interrupt INT0 ~ INT1, RXD pin, T0 pin, T1 pin and PCA input pins—CCP0 pin and CCP1 pin. When it is woken-up by RESET, the program will execute from the address 0x0000. Be carefully to keep RESET pin active for at least 10ms in order for a stable clock. If it is woken-up from I/O, the CPU will rework through jumping to related interrupt service routine. Before the CPU rework, the clock is blocked and counted until 32768 in order for denouncing the unstable clock. To use I/O wake-up, interrupt-related registers have to be enabled and programmed accurately before power-down is entered. Pay attention to have at least one “NOP” instruction subsequent to the power-down instruction if I/O wake-up is used. When terminating Power-down by an interrupt, the wake up period is internally timed. At the negative edge on the interrupt pin, Power-Down is exited, the oscillator is restarted, and an internal timer begins counting. The internal clock will be allowed to propagate and the CPU will not resume execution until after the timer has reached internal counter full. After the timeout period, the interrupt service routine will begin. To prevent the interrupt from re-triggering, the interrupt service routine should disable the interrupt before returning. The interrupt pin should be held low until the device has timed out and begun executing. The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 us until after one of the following conditions has occured: Start of code execution(after any type of reset), or Exit from power-down mode.

The following circuit can timing wake up MCU from power down mode when external interrupt sources do not exist

![Circuit Diagram](image)

Operation step:
1. I/O ports are first configured to push-pull output(strong pull-up) mode
2. Written 1s into ports I/O ports
3. The above circuit will charge the capacitor C1
4. Written 0s into ports I/O ports, MCU will go into power-down mode
5. The above circuit will discharge. When the electricity of capacitor C1 has been discharged less than 0.8V, external interrupt INTx pin will generate a falling edge and wake up MCU from power-down mode automatically.
The following example C program demonstrates that power-down mode be woken-up by external interrupt.

```c
#include <reg51.h>
#include <intrins.h>

sbit Begin_LED = P1^2; //Begin-LED indicator indicates system start-up
unsigned char Is_Power_Down = 0; //Set this bit before go into Power-down mode
sbit Is_Power_Down_LED_INT0 = P1^7; //Power-Down wake-up LED indicator on INT0
sbit Not_Power_Down_LED_INT0 = P1^6; //Not Power-Down wake-up LED indicator on INT0
sbit Is_Power_Down_LED_INT1 = P1^5; //Power-Down wake-up LED indicator on INT1
sbit Not_Power_Down_LED_INT1 = P1^4; //Not Power-Down wake-up LED indicator on INT1
sbit Power_Down_Wakeup_Pin_INT0 = P3^2; //Power-Down wake-up pin on INT0
sbit Power_Down_Wakeup_Pin_INT1 = P3^3; //Power-Down wake-up pin on INT1
sbit Normal_Work_Flashing_LED = P1^3; //Normal work LED indicator

void Normal_Work_Flashing (void);
void INT_System_init (void);
void INT0_Routine (void);
void INT1_Routine (void);

void main (void)
{
    unsigned char j = 0;
    unsigned char wakeup_counter = 0;
    Begin_LED = 0; //clear interrupt wakeup counter variable wakeup_counter
    INT_System_init ( ); //system start-up LED
    while(1)
    {
        P2 = wakeup_counter;
        wakeup_counter++;
        for(j=0; j<2; j++)
        {
            Normal_Work_Flashing( ); //System normal work
        }
    }
}
```

Is_Power_Down = 1;  //Set this bit before go into Power-down mode
PCON    = 0x02;  //after this instruction, MCU will be in power-down mode
            //external clock stop
            _nop_( );
            _nop_( );
            _nop_( );
            _nop_( );
}
}

void  INT_System_init (void)
{
    IT0   = 0;   /* External interrupt 0, low electrical level triggered */
    // IT0 = 1;   /* External interrupt 0, negative edge triggered */
    EX0   = 1;   /* Enable external interrupt 0 */
    IT1   = 0;   /* External interrupt 1, low electrical level triggered */
    // IT1 = 1;   /* External interrupt 1, negative edge triggered */
    EX1   = 1;   /* Enable external interrupt 1 */
    EA    = 1;   /* Set Global Enable bit */
}

void  INT0_Routine (void) interrupt 0
{
    if (Is_Power_Down)
    {
        //Is_Power_Down ==1;  /* Power-Down wakeup on INT0 */
        Is_Power_Down = 0;
        Is_Power_Down_LED_INT0 = 0;
        /*open external interrupt 0 Power-Down wake-up LED indicator */
        while (Power_Down_Wakeup_Pin_INT0 == 0)
        {
            /* wait higher */
        }
        Is_Power_Down_LED_INT0 = 1;  /* close external interrupt 0 Power-Down wake-up LED indicator */
    }
    else
    {
        Not_Power_Down_LED_INT0 = 0;  /* open external interrupt 0 normal work LED */
        while (Power_Down_Wakeup_Pin_INT0 ==0)
        {
            /* wait higher */
        }
        Not_Power_Down_LED_INT0 = 1;  /* close external interrupt 0 normal work LED */
    }
}
void INT1_Routine (void) interrupt 2
{
  if (Is_Power_Down)
  {
    //Is_Power_Down ==1;  /* Power-Down wakeup on INT1 */
    Is_Power_Down = 0;
    Is_Power_Down_LED_INT1= 0;
    /*open external interrupt 1 Power-Down wake-up LED indicator */
    while (Power_Down_Wakeup_Pin_INT1 == 0)
    {
      /* wait higher */
    }
    Is_Power_Down_LED_INT1 = 1;  /* close external interrupt 1 Power-Down wake-up LED indicator */
  }
  else
  {
    Not_Power_Down_LED_INT1 = 0;  /* open external interrupt 1 normal work LED */
    while (Power_Down_Wakeup_Pin_INT1 ==0)
    {
      /* wait higher */
    }
    Not_Power_Down_LED_INT1 = 1;  /* close external interrupt 1 normal work LED */
  }
}

void delay (void)
{
  unsigned int     j = 0x00;
  unsigned int     k = 0x00;
  for (k=0; k<2; ++k)
  {
    for (j=0; j<=30000; ++j)
    {
      _nop_( );
      _nop_( );
      _nop_( );
      _nop_( );
      _nop_( );
      _nop_( );
      _nop_( );
    }
  }
}
void Normal_Work_Flashing (void)
{
    Normal_Work_Flashing_LED = 0;
    delay ( );
    Normal_Work_Flashing_LED = 1;
    delay ( );
}

The following program also demonstrates that power-down mode or idle mode be woken-up by external interrupt, but is written in assembly language rather than C language.

;************************************************************
;Wake Up Idle and Wake Up Power Down
;************************************************************
ORG 0000H
AJMP MAIN
ORG 0003H
int0_interrupt:
    CLR P1.7   ;open P1.7 LED indicator
    ACALL delay   ;delay in order to observe
    CLR EA    ;clear global enable bit, stop all interrupts
    RETI

ORG 0013H
int1_interrupt:
    CLR P1.6   ;open P1.6 LED indicator
    ACALL delay   ;;delay in order to observe
    CLR EA    ;clear global enable bit, stop all interrupts
    RETI

ORG 0100H
delay:
    CLR A
    MOV R0, A
    MOV R1, A
    MOV R2, #02

delay_loop:
    DJNZ R0, delay_loop
    DJNZ R1, delay_loop
    DJNZ R2, delay_loop
    RET
main:
  MOV  R3,  #0  ;P1 LED increment mode changed
  ;start to run program

main_loop:
  MOV  A,  R3
  CPL  A
  MOV  P1,  A
  ACALL  delay
  INC  R3

  MOV  A,  R3
  SUBB  A,  #18H
  JC  main_loop

  MOV  P1,  #0FFH  ;close all LED, MCU go into power-down mode

  CLR  IT0  ;low electrical level trigger external interrupt 0
  ;  SETB  IT0  ;negative edge trigger external interrupt 0
  SETB  EX0  ;enable external interrupt 0

  CLR  IT1  ;low electrical level trigger external interrupt 1
  ;  SETB  IT1  ;negative edge trigger external interrupt 1
  SETB  EX1  ;enable external interrupt 1

  SETB  EA  ;set the global enable
  ;if don't so, power-down mode cannot be wake up

;MCU will go into idle mode or power-down mode after the following instructions
  MOV  PCON,  #00000010B  ;Set PD bit, power-down mode (PD = PCON.1)
  ;  NOP
  ;  NOP
  ;  NOP
  ;  MOV  PCON,  #00000001B  ;Set IDL bit, idle mode (IDL = PCON.0)

  MOV  P1,  #0DFH  ;1101,1111
  NOP
  NOP
  NOP
  WAIT1:
  SJMP  WAIT1  ;dynamically stop

END
2.3 RESET Control

In STC12C5A60S2, there are 6 sources to generate internal reset. They are RESET (P4.7) pin, On-chip power-on-reset, Watch-Dog-Timer, software reset, On-chip MAX810 POR timing delay and low-voltage detection (P4.6).

2.3.1 Reset pin

The P4.7 pin, if configured as RESET pin function (default), which is the input to Schmitt Trigger, is input pin for chip reset. A level change of RESET pin have to keep at least 24 cycles plus 10us in order for CPU internal sampling use.

STC12C5A60S2 series MCU add secondary RESET function (RST2/P4.6). When system frequency is up to 12MHz, the secondary reset function is recommended to use.
2.3.2 Power-On Reset (POR)

When VCC drops below the detection threshold of POR circuit, all of the logic circuits are reset.

When VCC goes back up again, an internal reset is released automatically after a delay of 32768 clocks. The nominal POR detection threshold is around 1.9V for 3V device and 3.3V for 5V device.

The Power-On flag, POF/PCON.4, is set by hardware to denote the VCC power has ever been less than the POR voltage. And, it helps users to check if the start of running of the CPU is from power-on or from hardware reset (RST-pin reset), software reset or Watchdog Timer reset. The POF bit should be cleared by software.

**PCON register (Power Control Register)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
<td>IDL</td>
</tr>
</tbody>
</table>

LVDF : Pin Low-Voltage Flag. Once low voltage condition is detected (VCC power is lower than LVD voltage), it is set by hardware (and should be cleared by software).

POF : Power-On flag. It is set by power-off-on action and can only cleared by software.

2.3.3 Watch-Dog-Timer

The watch dog timer in STC12C5A60S2 consists of an 8-bit pre-scaler timer and an 15-bit timer. The timer is one-time enabled by setting EN_WDT(WDT_CONTR.5). Clearing EN_WDT can stop WDT counting. When the WDT is enabled, software should always reset the timer by writing 1 to CLR_WDT bit before the WDT overflows. If STC12C5A60S2 series MCU is out of control by any disturbance, that means the CPU can not run the software normally, then WDT may miss the "writing 1 to CLR_WDT" and overflow will come. An overflow of Watch-Dog-Timer will generate a internal reset.

![WDT Structure](image-url)
WDT_CONTR: Watch-Dog-Timer Control Register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>WDT_FLAG</td>
<td>-</td>
<td>EN_WDT</td>
<td>CLR_WDT</td>
<td>IDLE_WDT</td>
<td>PS2</td>
<td>PS1</td>
<td>PS0</td>
</tr>
</tbody>
</table>

WDT_FLAG: WDT reset flag.
- 0: This bit should be cleared by software.
- 1: When WDT overflows, this bit is set by hardware to indicate a WDT reset happened.

EN_WDT: Enable WDT bit. When set, WDT is started.
CLR_WDT: WDT clear bit. When set, WDT will recount. Hardware will automatically clear this bit.
IDLE_WDT: WDT IDLE mode bit. When set, WDT is enabled in IDLE mode. When clear, WDT is disabled in IDLE.

PS2, PS1, PS0: WDT Pre-scale value set bit.
Pre-scale value of Watchdog timer is shown as the bellowed table:

<table>
<thead>
<tr>
<th>PS2</th>
<th>PS1</th>
<th>PS0</th>
<th>Pre-scale</th>
<th>WDT overflow Time @20MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>39.3 mS</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>78.6 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8</td>
<td>157.3 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>314.6 mS</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>32</td>
<td>629.1 mS</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>64</td>
<td>1.25 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>128</td>
<td>2.5 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>256</td>
<td>5 S</td>
</tr>
</tbody>
</table>

The WDT overflow time is determined by the following equation:

\[ \text{WDT overflow time} = \frac{(12 \times \text{Pre-scale} \times 32768)}{\text{SYSclk}} \]

The SYSclk is 20MHz in the table above.
If SYSclk is 12MHz, The WDT overflow time is:

\[ \text{WDT overflow time} = \frac{(12 \times \text{Pre-scale} \times 32768)}{12000000} = \text{Pre-scale} \times \frac{393216}{12000000} \]

WDT overflow time is shown as the bellowed table when SYSclk is 12MHz:

<table>
<thead>
<tr>
<th>PS2</th>
<th>PS1</th>
<th>PS0</th>
<th>Pre-scale</th>
<th>WDT overflow Time @12MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>65.5 mS</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>131.0 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8</td>
<td>262.1 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>524.2 mS</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>32</td>
<td>1.0485 S</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>64</td>
<td>2.0971 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>128</td>
<td>4.1943 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>256</td>
<td>8.3886 S</td>
</tr>
</tbody>
</table>
The following example is a assembly language program that demonstrates STC 1T Series MCU WDT.

; *------------------------------------------------------------------;
; /* --- STC MCU International Limited --------------------------------*/
; /* --- STC 1T Series MCU WDT Demo --------------------------------*/
; /* --- Mobile: (86)13922805190 -------------------------------------*/
; /* --- Fax: 86-755-82944243 ----------------------------------------*/
; /* --- Tel: 86-755-82948412 ----------------------------------------*/
; /* --- Web: www.STCMCU.com -----------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; *------------------------------------------------------------------;

; WDT overflow time = (12 × Pre-scale × 32768) / SYSclk

<table>
<thead>
<tr>
<th>PS2</th>
<th>PS1</th>
<th>PS0</th>
<th>Pre-scale</th>
<th>WDT Overflow Time @11.0592MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>71.1 mS</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
<td>142.2 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8</td>
<td>284.4 mS</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>16</td>
<td>568.8 mS</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>32</td>
<td>1.1377 S</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>64</td>
<td>2.2755 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>128</td>
<td>4.5511 S</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>256</td>
<td>9.1022 S</td>
</tr>
</tbody>
</table>

WDT overflow time is shown as the bellowed table when SYSclk is 11.0592MHz:

WDT_CONTR  EQU 0C1H  ;WDT address
WDT_TIME_LED  EQU P1.5  ;WDT overflow time LED on P1.5
;The WDT overflow time may be measured by the LED light time
WDT_FLAG_LED  EQU P1.7  ;WDT overflow reset flag LED indicator on P1.7

Last_WDT_Time_LED_Status EQU 00H  ;bit variable used to save the last statuts of WDT overflow time LED indicator

WDT reset time , the SYSclk is 18.432MHz
;Pre_scale_Word  EQU 00111100B  ;open WDT, Pre-scale value is 32, WDT overflow time=0.68S
;Pre_scale_Word  EQU 00111101B  ;open WDT, Pre-scale value is 64, WDT overflow time=1.36S
;Pre_scale_Word  EQU 00111110B  ;open WDT, Pre-scale value is 128, WDT overflow time=2.72S
;Pre_scale_Word  EQU 00111111B  ;open WDT, Pre-scale value is 256, WDT overflow time=5.44S
ORG  0000H
AJMP  MAIN

ORG  0100H

MAIN:

MOV  A,  WDT_CONTR ; detection if WDT reset
ANL  A,  #10000000B
JNZ  WDT_Reset

; WDT_CONTR.7=1, WDT reset, jump WDT reset subroutine
; WDT_CONTR.7=0, Power-On reset, cold start-up, the content of RAM is random

SETB  Last_WDT_Time_LED_Status ; Power-On reset
CLR  WDT_TIME_LED ; Power-On reset, open WDT overflow time LED

MOV  WDT_CONTR,  #Pre_scale_Word ; open WDT

WAIT1:

SJMP  WAIT1 ; wait WDT overflow reset

; WDT_CONTR.7=1, WDT reset, hot start-up, the content of RAM is constant and just like before reset

WDT_Reset:

CLR  WDT_FLAG_LED ; WDT reset, open WDT overflow reset flag LED indicator

JB  Last_WDT_Time_LED_Status,  Power_Off_WDT_TIME_LED
; when set Last_WDT_Time_LED_Status, close the corresponding LED indicator
; clear, open the corresponding LED indicator
; set WDT_TIME_LED according to the last status of WDT overflow time LED indicator

CLR  WDT_TIME_LED ; close the WDT overflow time LED indicator
CPL  Last_WDT_Time_LED_Status ; reverse the last status of WDT overflow time LED indicator

WAIT2:

SJMP  WAIT2 ; wait WDT overflow reset

Power_Off_WDT_TIME_LED:

SETB  WDT_TIME_LED ; close the WDT overflow time LED indicator
CPL  Last_WDT_Time_LED_Status ; reverse the last status of WDT overflow time LED indicator

WAIT3:

SJMP  WAIT3 ; wait WDT overflow reset

END
2.3.4 Software RESET

Writing an “1” to SWRST bit in IAP_CONTR register will generate an internal reset.

IAP_CONTR: ISP/IAP Control Register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>IAPEN</td>
<td>SWBS</td>
<td>SWRST</td>
<td>CMD_FAIL</td>
<td>-</td>
<td>WT2</td>
<td>WT1</td>
<td>WT0</td>
</tr>
</tbody>
</table>

IAPEN: ISP/IAP operation enable.
0: Global disable all ISP/IAP program/erase/read function.
1: Enable ISP/IAP program/erase/read function.

SWBS: software boot selection control.
0: Boot from main-memory after reset.
1: Boot from ISP memory after reset.

SWRST: software reset trigger control.
0: No operation
1: Generate software system reset. It will be cleared by hardware automatically.

CMD_FAIL: Command Fail indication for ISP/IAP operation.
0: The last ISP/IAP command has finished successfully.
1: The last ISP/IAP command fails. It could be caused since the access of flash memory was inhibited.

<table>
<thead>
<tr>
<th>Warm boot and Cold boot reset</th>
<th></th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset type</td>
<td>Reset source</td>
<td>System will reset to AP address 0000H and begin running user application program</td>
</tr>
<tr>
<td>Warm boot</td>
<td>WatchDog</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Reset Pin</td>
<td></td>
</tr>
<tr>
<td></td>
<td>20H → IAP_CONTR</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60H → IAP_CONTR</td>
<td></td>
</tr>
<tr>
<td>Cold boot</td>
<td>Power-on</td>
<td>System will reset to ISP address 0000H and begin running ISP monitor program, if not detected legitimate ISP command, system will software reset to the user program area automatically.</td>
</tr>
</tbody>
</table>

2.3.5 MAX810 power-on-reset delay

There is another on-chip POR delay circuit is integrated on STC12C5A60S2. This circuit is MAX810—special reset circuit and is controlled by configuring flash Option Register. Very long POR delay time – around 200ms will be generated by this circuit once it is enabled.
2.3.6 Low Voltage Detection

Besides the POR voltage, there is a higher threshold voltage: the Low Voltage Detection (LVD) voltage, 2.3V and 3.7V for STC12C5A60S2 and STC12LE5A60S2, respectively. When the VCC power drops down to the LVD voltage, the Low voltage Flag, LVD bit (PCON.5), will be set by hardware. (Note that during power-up, this flag will also be set, and the user should clear it by software for the following Low Voltage detecting.) This flag can also generate an interrupt if bit ELVD (IE.6) is set to 1.

Although the MCU can still work well between the ranges 1.9 ~ 2.3V (for STC12LE5A60S2) and 3.3 ~ 3.7V (for STC12C5A60S2), they are not safe enough for the IAP operation (especially writing Flash memory.)

Some SFRs related to Low voltage detection as shown below.

**PCON register** (Power Control Register)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
<td>IDL</td>
</tr>
</tbody>
</table>

LVDF : Pin Low-Voltage Flag. Once low voltage condition is detected (VCC power is lower than LVD voltage), it is set by hardware (and should be cleared by software).

**IE: Interrupt Enable Register**

<table>
<thead>
<tr>
<th>(MSB)</th>
<th>(LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EA</td>
<td>ELVD</td>
</tr>
</tbody>
</table>

Enable Bit = 1 enables the interrupt .
Enable Bit = 0 disables it .

EA (IE.7):  
disables all interrupts. if EA = 0 ,no interrupt will be acknowledged. if EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

ELVD (IE.6):  
Low volatge detection interrupt enable bit.

**IP: Interrupt Priority Register**

<table>
<thead>
<tr>
<th>(MSB)</th>
<th>(LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPCA</td>
<td>PLVD</td>
</tr>
</tbody>
</table>

Priority bit = 1 assigns high priority .
Priority bit = 0 assigns low priority.

PLVD (IP.6):  
Low voltage detection interrupt priority.
### WAKE_CLKO register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>PCAWAKEUP</td>
<td>RXD_PIN_IE</td>
<td>T1_PIN_IE</td>
<td>T0_PIN_IE</td>
<td>LVD_WAKE</td>
<td>BRTCKLO</td>
<td>T1CKLO</td>
<td>T0CKLO</td>
</tr>
</tbody>
</table>

**LVD_WAKE**: When set and the associated-LVD interrupt control registers is configured correctly, the CMPIN pin is enabled to wake up MCU from power-down state.

**BRTCKLO**: When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRG overflow rate divided by 2.

Typical application circuit, using EX_LVD pin achieve low-voltage-reset function, as shown below.

If power inputing source is 5V DC, then the reference application circuit as bellow: (Note: 7805 output 4V voltage and use R1 and R2 can achieve the low voltage reset function at 1.33V)

![Typical application circuit with 5V DC power source](image1)

If power inputing source is 220V AC, then the reference application circuit as bellow: (Note: 7805 output 8.5V voltage and use R1 and R2 can achieve the low voltage reset function at 1.33V)

![Typical application circuit with 220V AC power source](image2)

The program that demonstrates the External Low Voltage detection function on P4.6 as shown below:

```assembly
RUN_LED EQU P1.0 ;Program normal running LED indicator
ERROR_LED EQU P1.1 ;Error LED indicator
Hi_Volt_LED EQU P1.2 ;Normal voltage LED indicator
Power_On_LED EQU P1.3 ;Power-On LED indicator
Low_Volt_LED EQU P1.4 ;Low-Voltage LED indicator

ORG 0000H
AJMP MAIN

ORG 0100H

MAIN:
MOV SP, #070H ;Initialize stack pointer
SETB RUN_LED ;Demo program start to work
LCALL Delay ;delay
CLR RUN_LED ;Demo program start to work
LCALL Delay ;delay
SETB RUN_LED ;Demo program start to work
```

STC MCU Limited

website: www.STCMCU.com
MAIN1:

```
MOV   A,   PCON
JBC   ACC.5, Power_On_1
CLR ERROR_LED
SETB Power_On_LED
SETB Hi_Volt_LED
SETB Low_Volt_LED
```

ERROR:

```
LJMP  ERROR
```

Power_On_1:

```
SETB ERROR_LED
CLR Power_On_LED
SETB Hi_Volt_LED
SETB Low_Volt_LED
LCALL Delay ;delay
Continue_Read:
```
MOV   A, #11011111B
ANL   PCON, A
NOP
MOV   A, PCON
JBC   ACC.5, Low_Voltage
```

High_Voltage:

```
SETB ERROR_LED
SETB Power_On_LED
CLR Hi_Volt_LED
SETB Low_Volt_LED
LJMP Continue_Read
```

Low_Voltage:

```
SETB ERROR_LED
SETB Power_On_LED
CLR Hi_Volt_LED
SETB Low_Volt_LED
LJMP Continue_Read
```

Delay:

```
CLR A
MOV R0, A
MOV R1, A
MOV R2, #30H
```

Delay_Loop:

```
DJNZ R0, Delay_Loop
DJNZ R1, Delay_Loop
DJNZ R2, Delay_Loop
RET
END
```
Chapter 3. Memory Organization

The STC12C5A60S2 series MCU has separate address space for Program Memory and Data Memory. The logical separation of program and data memory allows the data memory to be accessed by 8-bit addresses, which can be quickly stored and manipulated by the CPU.

Program memory (ROM) can only be read, not written to. In the STC12C5A60S2 series, all the program memory are on-chip Flash memory, and without the capability of accessing external program memory because of no External Access Enable (/EA) and Program Store Enable (/PSEN) signals designed.

Data memory occupies a separate address space from program memory. In the 12C5A60S2 series, there are 256 bytes of internal scratch-pad RAM and 1024 bytes of on-chip expanded RAM(XRAM).

3.1 Program Memory

Program memory is the memory which stores the program codes for the CPU to execute. There is 8/16/20/32/40/48/52/56/62K-bytes of flash memory embedded for program and data storage. The design allows users to configure it as like there are three individual partition banks inside. They are called AP(application program) region, IAP (In-Application-Program) region and ISP (In-System-Program) boot region. AP region is the space that user program is resided. IAP(In-Application-Program) region is the nonvolatile data storage space that may be used to save important parameters by AP program. In other words, the IAP capability of STC12C5A60S2 provides the user to read/write the user-defined on-chip data flash region to save the needing in use of external EEPROM device. ISP boot region is the space that allows a specific program we calls “ISP program” is resided. Inside the ISP region, the user can also enable read/write access to a small memory space to store parameters for specific purposes. Generally, the purpose of ISP program is to fulfill AP program upgrade without the need to remove the device from system. STC12C5A60S2 hardware catches the configuration information since power-up duration and performs out-of-space hardware-protection depending on pre-determined criteria. The criteria is AP region can be accessed by ISP program only, IAP region can be accessed by ISP program and AP program, and ISP region is prohibited access from AP program and ISP program itself. But if the “ISP data flash is enabled”, ISP program can read/write this space. When wrong settings on ISP-IAP SFRs are done, The “out-of-space” happens and STC12C5A60S2 follows the criteria above, ignore the trigger command.

After reset, the CPU begins execution from the location 0000H of Program Memory, where should be the starting of the user’s application code. To service the interrupts, the interrupt service locations (called interrupt vectors) should be located in the program memory. Each interrupt is assigned a fixed location in the program memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose program memory.

The interrupt service locations are spaced at an interval of 8 bytes: 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.
3.2 Data Memory

3.2.1 On-chip Scratch-Pad RAM

Just the same as the conventional 8051 micro-controller, there are 256 bytes of SRAM data memory plus 128 bytes of SFR space available on the STC12C5A60S2. The lower 128 bytes of data memory may be accessed through both direct and indirect addressing. The upper 128 bytes of data memory and the 128 bytes of SFR space share the same address space. The upper 128 bytes of data memory may only be accessed using indirect addressing. The 128 bytes of SFR can only be accessed through direct addressing. The lowest 32 bytes of data memory are grouped into 4 banks of 8 registers each. Program instructions call out these registers as R0 through R7. The RS0 and RS1 bits in PSW register (refer to section 3.2.4) select which register bank is in use. Instructions using register addressing will only access the currently specified bank. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing. The next 16 bytes (20H~2FH) above the register banks form a block of bit-addressable memory space. The 80C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing while the Upper 128 can only be accessed by indirect addressing. SFRs include the Port latches, timers, peripheral controls, etc. These registers can only be accessed by direct addressing. Sixteen addresses in SFR space are both byte- and bit-addressable. The bit-addressable SFRs are those whose address ends in 0H or 8H.

3.2.2 Auxiliary RAM

There are 1024 bytes of additional data RAM available on STC12C5A60S2. They may be accessed by the instructions MOVX @Ri or MOVX @DPTR. A control bit – EXTRAM located in AUXR.1 register (refer to section 3.2.4) is to control access of auxiliary RAM. When set, disable the access of auxiliary RAM. When clear (EXTRAM=0), this auxiliary RAM is the default target for the address range from 0x0000 to 0x03FF and can be indirectly accessed by move external instruction, “MOVX @Ri” and “MOVX @DPTR”. If EXTRAM=0 and the target address is over 0x03FF, switches to access external RAM automatically. When EXTRAM=0, the content in DPH is ignored when the instruction MOVX @Ri is executed.

For KEIL-C51 compiler, to assign the variables to be located at Auxiliary RAM, the “pdata” or “xdata” definition should be used. After being compiled, the variables declared by “pdata” and “xdata” will become the memories accessed by “MOVX @Ri” and “MOVX @DPTR”, respectively. Thus the STC12C5A60S2 hardware can access them correctly.
3.2.3 External RAM

There is 64K-byte addressing space available for STC12C5A60S2 to access external data RAM. Just the same as the design in the conventional 8051, the port – P2, P0, ALE, P3.6 and P3.7 have alterative function for external data RAM access. In addition, a new register BUS_SPEED (address: 0xA1) is design to control the access timing of "MOVX" instruction. In BUS_SPEED register, {ALES1 and ALES0} is to stretch the setup time and hold time with respect to ALE negative edge and {RW2, RW1, RW0} is to stretch the pulse width of /WR(P3.6) and /RD(P3.7). By using BUS_SPEED to change the instruction cycle time, STC12C5A60S2 can conformed to communicate with both of fast and slow peripheral devices without loss of communication efficiency.

3.2.4 Special Function Register for RAM

Some SFRs related to RAM are shown as follow.

For fast data movement, STC12C5A60S2 supports two data pointers. They share the same SFR address and are switched by the register bit – DPS.
PSW register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CY</td>
<td>AC</td>
<td>F0</td>
<td>RS1</td>
<td>RS0</td>
<td>OV</td>
<td>F1</td>
<td>P</td>
</tr>
</tbody>
</table>

CY: Carry flag.
AC: Auxilliary Carry Flag (For BCD operations)
F0: Flag 0.(Available to the user for general purposes)
RS1: Register bank select control bit 1.
RS0: Register bank select control bit 0.
OV: Overflow flag.
F1: Flag 1. User-defined flag.
P: Parity flag.

AUXR register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
<td>S2SMOD</td>
<td>BRTx12</td>
<td>EXTRAM</td>
<td>S1BRS</td>
</tr>
</tbody>
</table>

T0x12
0: The clock source of Timer 0 is SYSclk/12.
1: The clock source of Timer 0 is SYSclk.

T1x12
0: The clock source of Timer 1 is SYSclk/12.
1: The clock source of Timer 1 is SYSclk.

UART_M0x6
0: The baud-rate of UART in mode 0 is SYSclk/12.
1: The baud-rate of UART in mode 0 is SYSclk/2.

BRTR
0: The baud-rate generator of UART2 (S2) is stopped.
1: The baud-rate generator of UART2 (S2) is enabled.

S2SMOD
0: Default.
1: The baud-rate UART2 (S2) is doubled.

BRTx12
0: The baud-rate generator is incremented every 12 system clocks.
1: The baud-rate generator is incremented every system clock.

EXTRAM
0: On-chip auxiliary RAM is enabled and located at the address 0x0000 to 0x03FF.
   For address over 0x03FF, off-chip external RAM becomes the target automatically.
1: On-chip auxiliary RAM is always disabled.

S1BRS
0: Default.
1: Timer 1 is replaced by the baud-rate generator of UART2 for use of the enhanced UART. In other words, timer 1 is released to use in other functions, and therefore enhanced UART and UART2 share the baud-rate generator in UART2.
**AUXR1 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
</tr>
</tbody>
</table>

**PCA_P4**
- 0 : Default.
- 1 : The PCA function in P1 [4:2] is switched to P4[3:1].

**SPI_P4**
- 0 : Default.
- 1 : The SPI function in P1[7:4] is redirected to P4[3:0].

**S2_P4**
- 0 : Default.
- 1 : The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].

**GF2** : General Flag. It can be used by software.

**ADJR**
- 0 : The 10-bit conversion result of ADC is arranged as \{ADC[7:0], ADCVL[1:0]\}.
- 1 : The 10-bit conversion result is right-justified, \{ADCV[1:0], ADCVL[7:0]\}.

**DPS**
- 0 : Default.
- 1 : The secondary DPTR is switched to use.
BUS_SPEED register

<table>
<thead>
<tr>
<th>bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>ALES1</td>
<td>ALES0</td>
<td>-</td>
<td>RWS2</td>
<td>RWS1</td>
<td>RWS0</td>
</tr>
</tbody>
</table>

{ALES1 and ALES0}:
00: The P0 address setup time and hold time to ALE negative edge is one clock cycle.
01: The P0 address setup time and hold time to ALE negative edge is two clock cycles.
10: The P0 address setup time and hold time to ALE negative edge is three clock cycles. (default)
11: The P0 address setup time and hold time to ALE negative edge is four clock cycles.

{RWS2, RWS1, RWS0}:
000: The MOVX read/write pulse is 1 clock cycle.
001: The MOVX read/write pulse is 2 clock cycles.
010: The MOVX read/write pulse is 3 clock cycles.
011: The MOVX read/write pulse is 4 clock cycles. (default)
100: The MOVX read/write pulse is 5 clock cycles.
101: The MOVX read/write pulse is 6 clock cycles.
110: The MOVX read/write pulse is 7 clock cycles.
111: The MOVX read/write pulse is 8 clock cycles.

When the target is on-chip auxiliary RAM, the setting on BUS_SPEED register is discarded by hardware.

Timing diagram for MOVX @DPTR, A without stretch

![Timing Diagram](image-url)
Timing diagram for MOVX A, @DPTR without stretch

Clock

P2
High-byte address
High-byte address

P0
Low-byte Address
Data
Port weak-pullup
Low-byte Address
Data
Port weak-pullup

ALE

/RD
(P3.7)

MOVX read cycle
MOVX read cycle

Timing diagram for MOVX @DPTR, A with stretch \{RWS2,RWS1,RWS0\} = 3'b111
Twr = 8 clock cycles (Twr is stretched by 7 cycles).

Clock

P2

P0
Low-byte Address
Data for writing

ALE

/WR
(P3.6)

MOVX write cycle

Twr = (1+7) cycles

Timing diagram for MOVX @DPTR, A with stretch \{RWS2,RWS1,RWS0\} = 3'b111 and
\{ALES1,ALES0\} = 2'b11
The Trd is stretched by 7, so Twr = 8 clock cycles. TALES is stretched by 3, so TALES = 4 clock
cycles and TALEH = 4 clock cycles.

Clock

P2

P0
Low-byte Address

ALE

/RD
(P3.7)

ALE setup time (1+3 cycles)
ALE hold time (1+3 cycles)

Trd = (1+7) cycles

MOVX read cycle
An example program for internal expanded RAM demo of STC12C5A60S2:

```c
#include<reg51.h>
#include<intrins.h>   /* use _nop_( ) function */

sfr AUXR = 0x8e;

sbit ERROM_LED = P1^5;
sbit OK_LED = P1^7;

void main ( )
{
    unsigned int array_point = 0;

    /*Test-array: Test_array_one[512], Test_array_two[512] */
    unsigned char xdata Test_array_one[512] =
    {
        0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07,
        0x08, 0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f,
        0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17,
        0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e, 0x1f,
        0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27,
        0x28, 0x29, 0x2a, 0x2b, 0x2c, 0x2d, 0x2e, 0x2f,
        0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37,
        0x38, 0x39, 0x3a, 0x3b, 0x3c, 0x3d, 0x3e, 0x3f,
        0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47,
        0x48, 0x49, 0x4a, 0x4b, 0x4c, 0x4d, 0x4e, 0x4f,
        0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57,
        0x58, 0x59, 0x5a, 0x5b, 0x5c, 0x5d, 0x5e, 0x5f,
        0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67,
        0x68, 0x69, 0x6a, 0x6b, 0x6c, 0x6d, 0x6e, 0x6f,
        0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77,
        0x78, 0x79, 0x7a, 0x7b, 0x7c, 0x7d, 0x7e, 0x7f,
        0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87,
        0x88, 0x89, 0x8a, 0x8b, 0x8c, 0x8d, 0x8e, 0x8f,
        0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97,
        0x98, 0x99, 0x9a, 0x9b, 0x9c, 0x9d, 0x9e, 0x9f,
        0xa0, 0xa1, 0xa2, 0xa3, 0xa4, 0xa5, 0xa6, 0xa7,
        0xa8, 0xa9, 0xaa, 0xab, 0xac, 0xad, 0xae, 0xaf,
    };
```
0xb0, 0xb1, 0xb2, 0xb3, 0xb4, 0xb5, 0xb6, 0xb7, 0xb8, 0xb9, 0xba, 0xbb, 0xbc, 0xbd, 0xbe, 0xbf, 0xc0, 0xc1, 0xc2, 0xc3, 0xc4, 0xc5, 0xc6, 0xc7, 0xc8, 0xc9, 0xca, 0xcb, 0xcc, 0xcd, 0xce, 0xcf, 0xd0, 0xd1, 0xd2, 0xd3, 0xd4, 0xd5, 0xd6, 0xd7, 0xd8, 0xd9, 0xda, 0xdb, 0xdc, 0xdd, 0xde, 0xdf, 0xe0, 0xe1, 0xe2, 0xe3, 0xe4, 0xe5, 0xe6, 0xe7, 0xe8, 0xe9, 0xea, 0xeb, 0xec, 0xed, 0xee, 0xef, 0xf0, 0xf1, 0xf2, 0xf3, 0xf4, 0xf5, 0xf6, 0xf7, 0xf8, 0xf9, 0xfa, 0xfb, 0xfc, 0xfd, 0xfe, 0xff,

unsigned char xdata Test_array_two[512] =
{
  0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, 0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e, 0x1f, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2a, 0x2b, 0x2c, 0x2d, 0x2e, 0x2f, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3a, 0x3b, 0x3c, 0x3d, 0x3e, 0x3f, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4a, 0x4b, 0x4c, 0x4d, 0x4e, 0x4f, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5a, 0x5b, 0x5c, 0x5d, 0x5e, 0x5f, 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6a, 0x6b, 0x6c, 0x6d, 0x6e, 0x6f, 0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77, 0x78, 0x79, 0x7a, 0x7b, 0x7c, 0x7d, 0x7e, 0x7f, 0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87, 0x88, 0x89, 0x8a, 0x8b, 0x8c, 0x8d, 0x8e, 0x8f, 0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97, 0x98, 0x99, 0x9a, 0x9b, 0x9c, 0x9d, 0x9e, 0x9f, 0xa0, 0xa1, 0xa2, 0xa3, 0xa4, 0xa5, 0xa6, 0xa7, 0xa8, 0xa9, 0xaa, 0xab, 0xac, 0xad, 0xae, 0xaf, 0xb0, 0xb1, 0xb2, 0xb3, 0xb4, 0xb5, 0xb6, 0xb7, 0xb8, 0xb9, 0xba, 0xbb, 0xbc, 0xbd, 0xbe, 0xbf, 0xc0, 0xc1, 0xc2, 0xc3, 0xc4, 0xc5, 0xc6, 0xc7, 0xc8, 0xc9, 0xca, 0xcb, 0xcc, 0xcd, 0xce, 0xcf, 0xd0, 0xd1, 0xd2, 0xd3, 0xd4, 0xd5, 0xd6, 0xd7, 0xd8, 0xd9, 0xda, 0xdb, 0xdc, 0xdd, 0xde, 0xdf, 0xe0, 0xe1, 0xe2, 0xe3, 0xe4, 0xe5, 0xe6, 0xe7, 0xe8, 0xe9, 0xea, 0xeb, 0xec, 0xed, 0xee, 0xef, 0xf0, 0xf1, 0xf2, 0xf3, 0xf4, 0xf5, 0xf6, 0xf7, 0xf8, 0xf9, 0xfa, 0xfb, 0xfc, 0xfd, 0xfe, 0xff,};
0x6f, 0x6e, 0x6d, 0x6c, 0x6b, 0x6a, 0x69, 0x68,
0x67, 0x66, 0x65, 0x64, 0x63, 0x62, 0x61, 0x60,
0x5f, 0x5e, 0x5d, 0x5c, 0x5b, 0x5a, 0x59, 0x58,
0x57, 0x56, 0x55, 0x54, 0x53, 0x52, 0x51, 0x50,
0x4f, 0x4e, 0x4d, 0x4c, 0x4b, 0x4a, 0x49, 0x48,
0x47, 0x46, 0x45, 0x44, 0x43, 0x42, 0x41, 0x40,
0x3f, 0x3e, 0x3d, 0x3c, 0x3b, 0x3a, 0x39, 0x38,
0x37, 0x36, 0x35, 0x34, 0x33, 0x32, 0x31, 0x30,
0x2f, 0x2e, 0x2d, 0x2c, 0x2b, 0x2a, 0x29, 0x28,
0x27, 0x26, 0x25, 0x24, 0x23, 0x22, 0x21, 0x20,
0x1f, 0x1e, 0x1d, 0x1c, 0x1b, 0x1a, 0x19, 0x18,
0x17, 0x16, 0x15, 0x14, 0x13, 0x12, 0x11, 0x10,
0x0f, 0x0e, 0x0d, 0x0c, 0x0b, 0x0a, 0x09, 0x08,
0x07, 0x06, 0x05, 0x04, 0x03, 0x02, 0x01, 0x00

};

ERROR_LED = 1;
OK_LED = 1;
for (array_point = 0; array_point<512; array_point++)
{
    if (Test_array_one[array_point] != Test_array_two[array_point])
    {
        ERROR_LED = 0;
        OK_LED = 1;
        break;
    }
    else{
        OK_LED = 0;
        ERROR_LED = 1;
    }
}
while (1);
Chapter 4. Configurable I/O Ports

4.1 I/O Port Configurations

All port pins on STC12C5A60S2 may be independently configured to one of four modes: quasi-bidirectional (standard 8051 port output), push-pull output, input-only or open-drain output. All port pins default to quasi-bidirectional after reset. Each one has a Schmitt-triggered input for improved input noise rejection.

P4.4, P4.5, P4.6 and P4.7 are located at the pins - PSEN, ALE, EA and RST of conventional 80C51. Pay attention that additional control bits on P4SW register are used to enable the I/O port functions of these pins. Prior to use them as I/O port, the users must set the corresponding bit to enable it.

4.1.1 Quasi-bidirectional I/O

Port pins in quasi-bidirectional output mode function similar to the standard 8051 port pins. A quasi-bidirectional port can be used as an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic high, it is weakly driven, allowing an external device to pull the pin low. When the pin outputs low, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the “very weak” pull-up, is turned on whenever the port register for the pin contains a logic “1”. This very weak pull-up sources a very small current that will pull the pin high if it is left floating.

A second pull-up, called the “weak” pull-up, is turned on when the port register for the pin contains a logic “1” and the pin itself is also at a logic “1” level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is pulled low by the external device, this weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin low under these conditions, the external device has to sink enough current to over-power the weak pull-up and pull the port pin below its input threshold voltage.

The third pull-up is referred to as the “strong” pull-up. This pull-up is used to speed up low-to-high transitions on a quasi-bidirectional port pin when the port register changes from a logic “0” to a logic “1”. When this occurs, the strong pull-up turns on for two CPU clocks, quickly pulling the port pin high.

![Quasi-bidirectional output diagram](image)
4.1.2 Push-pull Output

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port register contains a logic “1”. The push-pull mode may be used when more source current is needed from a port output. In addition, input path of the port pin in this configuration is also the same as quasi-bidirectional mode.

![Push-pull output diagram]

4.1.3 Input-only Mode

The input-only configuration is a Schmitt-triggered input without any pull-up resistors on the pin.

![Input-only Mode diagram]

4.1.4 Open-drain Output

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port pin when the port register contains a logic “0”. To use this configuration in application, a port pin must have an external pull-up, typically tied to VCC. The input path of the port pin in this configuration is the same as quasi-bidirectional mode.

![Open-drain output diagram]
4.2 I/O Port Registers

All port pins on STC12C5A60S2 may be independently configured by software to one of four types on a bit-by-bit basis, as shown in next Table. Two mode registers for each port select the output mode for each port pin.

Table: Configuration of I/O port mode.

<table>
<thead>
<tr>
<th>PxM1.n</th>
<th>PxM0.n</th>
<th>Port Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Quasi-bidirectional</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Push-Pull output</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Input Only (High-impedance)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Open-Drain Output</td>
</tr>
</tbody>
</table>

where \( x = 0 \sim 4 \) (port number), and \( n = 0 \sim 7 \) (port pin).

**P0 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P0.7</td>
<td>P0.6</td>
<td>P0.5</td>
<td>P0.4</td>
<td>P0.3</td>
<td>P0.2</td>
<td>P0.1</td>
<td>P0.0</td>
</tr>
</tbody>
</table>

P0 register could be bit-addressable. And P0.7~P0.0 coulde be set/cleared by CPU.

**P0M1 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P0M1.7</td>
<td>P0M1.6</td>
<td>P0M1.5</td>
<td>P0M1.4</td>
<td>P0M1.3</td>
<td>P0M1.2</td>
<td>P0M1.1</td>
<td>P0M1.0</td>
</tr>
</tbody>
</table>

**P0M0 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P0M0.7</td>
<td>P0M0.6</td>
<td>P0M0.5</td>
<td>P0M0.4</td>
<td>P0M0.3</td>
<td>P0M0.2</td>
<td>P0M0.1</td>
<td>P0M0.0</td>
</tr>
</tbody>
</table>

**P1 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P1.7</td>
<td>P1.6</td>
<td>P1.5</td>
<td>P1.4</td>
<td>P1.3</td>
<td>P1.2</td>
<td>P1.1</td>
<td>P1.0</td>
</tr>
</tbody>
</table>

P1 register could be bit-addressable and set/cleared by CPU. And P1.7~P1.0 coulde be set/cleared by CPU.

**P1M1 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P1M1.7</td>
<td>P1M1.6</td>
<td>P1M1.5</td>
<td>P1M1.4</td>
<td>P1M1.3</td>
<td>P1M1.2</td>
<td>P1M1.1</td>
<td>P1M1.0</td>
</tr>
</tbody>
</table>

**P1M0 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P1M0.7</td>
<td>P1M0.6</td>
<td>P1M0.5</td>
<td>P1M0.4</td>
<td>P1M0.3</td>
<td>P1M0.2</td>
<td>P1M0.1</td>
<td>P1M0.0</td>
</tr>
</tbody>
</table>

**P2 register**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P2.7</td>
<td>P2.6</td>
<td>P2.5</td>
<td>P2.4</td>
<td>P2.3</td>
<td>P2.2</td>
<td>P2.1</td>
<td>P2.0</td>
</tr>
</tbody>
</table>
### P2M1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P2M1.7</td>
<td>P2M1.6</td>
<td>P2M1.5</td>
<td>P2M1.4</td>
<td>P2M1.3</td>
<td>P2M1.2</td>
<td>P2M1.1</td>
<td>P2M1.0</td>
</tr>
</tbody>
</table>

### P2M0 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P2M0.7</td>
<td>P2M0.6</td>
<td>P2M0.5</td>
<td>P2M0.4</td>
<td>P2M0.3</td>
<td>P2M0.2</td>
<td>P2M0.1</td>
<td>P2M0.0</td>
</tr>
</tbody>
</table>

### P3 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P3.7</td>
<td>P3.6</td>
<td>P3.5</td>
<td>P3.4</td>
<td>P3.3</td>
<td>P3.2</td>
<td>P3.1</td>
<td>P3.0</td>
</tr>
</tbody>
</table>

P3 register could be bit-addressable and set/cleared by CPU. And P3.7~P3.0 could be set/cleared by CPU.

### P3M1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P3M1.7</td>
<td>P3M1.6</td>
<td>P3M1.5</td>
<td>P3M1.4</td>
<td>P3M1.3</td>
<td>P3M1.2</td>
<td>P3M1.1</td>
<td>P3M1.0</td>
</tr>
</tbody>
</table>

### P3M0 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P3M0.7</td>
<td>P3M0.6</td>
<td>P3M0.5</td>
<td>P3M0.4</td>
<td>P3M0.3</td>
<td>P3M0.2</td>
<td>P3M0.1</td>
<td>P3M0.0</td>
</tr>
</tbody>
</table>

### P4 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P4.7</td>
<td>P4.6</td>
<td>P4.5</td>
<td>P4.4</td>
<td>P4.3</td>
<td>P4.2</td>
<td>P4.1</td>
<td>P4.0</td>
</tr>
</tbody>
</table>

P4 register could be bit-addressable and set/cleared by CPU. And P4.7~P1.0 could be set/cleared by CPU. P4.5 is an alternated function on ALE pin.

### P4M1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P4M1.7</td>
<td>P4M1.6</td>
<td>P4M1.5</td>
<td>P4M1.4</td>
<td>P4M1.3</td>
<td>P4M1.2</td>
<td>P4M1.1</td>
<td>P4M1.0</td>
</tr>
</tbody>
</table>

### P4M0 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>P4M0.7</td>
<td>P4M0.6</td>
<td>P4M0.5</td>
<td>P4M0.4</td>
<td>P4M0.3</td>
<td>P4M0.2</td>
<td>P4M0.1</td>
<td>P4M0.0</td>
</tr>
</tbody>
</table>
P5 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>P5.3</td>
</tr>
</tbody>
</table>

P5M1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td>P5M1.3</td>
<td>P5M1.2</td>
<td>P5M1.1</td>
<td>P5M1.0</td>
<td></td>
</tr>
</tbody>
</table>

P5M0 register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td>P5M0.3</td>
<td>P5M0.2</td>
<td>P5M0.1</td>
<td>P5M0.0</td>
<td></td>
</tr>
</tbody>
</table>

P4SW register

<table>
<thead>
<tr>
<th>bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>LVD_P4.6</td>
<td>ALE_P4.5</td>
<td>NA_P4.4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

LVD_P4.6: Set this bit to switch CMPIN to become P4.6. (Pin Location: Convention 80C51’s EA)
- 0: the pin functions as the input channel of internal LVD analog comparator.
  All pin leakage current has been cut off.
- 1: the pin functions as P4.6.

ALE_P4.5: Set this bit to switch ALE to become P4.5. (Pin Location: Convention 80C51’s ALE)
- 0: the pin functions as ALE output for use in MOVX instruction only.
- 1: the pin functions as P4.5.

NA_P4.4: Set this bit to enable P4.4. (Pin Location: Convention 80C51’s PSEN)
- 0: the pin is always kept at weak-high state.
- 1: the pin functions as P4.4

AUXR1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
<td></td>
</tr>
</tbody>
</table>

PCA_P4
- 0: Default.
- 1: The PCA function in P1[4:2] is switched to P4[3:1].

SPI_P4
- 0: Default.
- 1: The SPI function in P1[7:4] is redirected to P4[3:0].

S2_P4
- 0: Default.
- 1: The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].
4.3 I/O port application notes

Traditional 8051 access I/O (signal transition or read status) timing is 12 clocks, STC12C5A60S2 series MCU is 4 clocks. When you need to read an external signal, if internal output a rising edge signal, for the traditional 8051, this process is 12 clocks, you can read at once, but for STC12C5A60S2 series MCU, this process is 4 clocks, when internal instructions is complete but external signal is not ready, so you must delay 1~2 nop operation.

When MCU is connected to a SPI or I2C or other open-drain peripherals circuit, you need add a 10K pull-up resistor.

Some IO port connected to a PNP transistor, but no pul-up resistor. The correct access method is IO port pull-up resistor and transistor base resistor should be consistent, or IO port is set to a strongly push-pull output mode.

Using IO port drive LED directly or matrix key scan, needs add a 470ohm to 1Kohm resistor to limit current.

4.4 I/O port application

4.4.1 Typical transistor control circuit

If I/O is configed as “weak” pull-up, you should add a external pull-up (3.3K~10K ohm). If no pull-up resistor R1, proposal to add a 15K ohm series resistor at least or config I/O as “push-pull” mode.

4.4.2 Typical diode control circuit

For weak pull-up / quasi-bidirectional I/O, use sink current drive LED, current limiting resistor as greater than 1K ohm, minimum not less than 470 ohm.

For push-pull / strong pull-up I/O, use drive current drive LED.
4.4.3 3V/5V hybrid system

When STC12C5A60S2 series 5V MCU connect to 3V peripherals. To prevent the device can not afford to 5V voltage, the corresponding I/O is set to open drain mode, disconnect the internal pull-up resistor, the corresponding IO port add 10K ohm external pull-up resistor to the 3V device VCC, so high To 3V, low to 0V, which can proper functioning

When STC12C5A60S2 series 3V MCU connect to 5V peripherals. To prevent the MCU can not afford to 5V voltage, if the corresponding IO port as input port, the port may be in an isolation diode in series, isolated high-voltage part, the external signal is higher than MCU operating voltage, the diode cut-off, IO I have been pulled high by the internal pull-up resistor; when the external signal is low, the diode conduction, IO port voltage is limited to 0.7V, it’s low signal to MCU.

![MCU I/O External Signal Diagram](image)

4.4.4 How to make I/O port low after MCU reset

Traditional 8051 MCU power-on reset, the general IO port are weak pull-high output, while many practical applications require IO port remain low level after power-on reset, otherwise the system malfunction would be generated. For STC12C5A60S2 series MCU, IO port can add a pull-down resistor (1K/2K/3K), so that when power-on reset, although a weak internal pull-up to make MCU output high, but because of the limited capacity of the internal pull-up, it can not pull-high the pad, so this IO port is low level after power-on reset. If the I/O port need to drive high, you can set the IO model as the push-pull output mode, while the push-pull mode the drive current can be up to 20mA, so it can drive this I/O high.

![I/O Status Diagram](image)

4.4.5 I/O status while PWM outputing

When I/O is used as PWM port, it’s status as bellow:

<table>
<thead>
<tr>
<th>Before PWM output</th>
<th>While PWM outputing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quasi-bidirectional</td>
<td>Push-Pull (Strong pull-high need 1K~10K limiting resistor)</td>
</tr>
<tr>
<td>Push-Pull</td>
<td>Push-Pull (Strong pull-high need 1K~10K limiting resistor)</td>
</tr>
<tr>
<td>Input only (Floating)</td>
<td>Invalid</td>
</tr>
<tr>
<td>Open-drain</td>
<td>Open-drain</td>
</tr>
</tbody>
</table>
4.4.6 I/O drive LED application circuit

I/O dynamic scan driver 4 groups of digital tube Cathode circuit

I/O dynamic scan driver 4 groups of digital tube anode circuit
4.4.7 I/O immediately drive LED application circuit

How to light on the LCD pixels:
When the pixels corresponding COM-side and SEG-side voltage difference is greater than 1/2VCC, this pixel is lit, otherwise off.

Contrl SEG-side (Segment):
I/O direct drive Segment lines, control Segment output high-level (VCC) or low-level (0V).

Contrl COM-side (Common):
I/O port and two 100K dividing resistors jointly controlled Common line, when the IO output "0", the Common-line is low level (0V), when the IO push-pull output "1", the Common line is high level (VCC), when IO as high-impedance input, the Common line is 1/2VCC.

Before MCU enter Power Down mode, the I/O output high level, then Common side will have no leakage current.
### 4.4.8 Using A/D Conversion to scan key application circuit

This circuit can achieve a single key or combin key scan, resistance need to configure the actual needs.

This circuit uses 10 keys spaced partial pressure, for each key, range of allowed error is +/-0.25V, it can effectively avoid failure of key detection because of resistance or temperature drift. If the requested key detection is more stable and reliable, it can reduce the number of buttons, to relax the voltage range of each key.
### Chapter 5 Instruction System

#### 5.1 Special Function Registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Bit</th>
<th>Non Bit Addressable</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F8H</td>
<td>CH</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0F0H</td>
<td>B</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0E8H</td>
<td>CL</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0E0H</td>
<td>ACC</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0D8H</td>
<td>CCON</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0D0H</td>
<td>PSW</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0C8H</td>
<td>P5</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0C0H</td>
<td>P4</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0B8H</td>
<td>IP</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0B0H</td>
<td>P3</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0A8H</td>
<td>IE</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>0A0H</td>
<td>P2</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>098H</td>
<td>SCON</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>090H</td>
<td>P1</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>088H</td>
<td>TCON</td>
<td>0/8</td>
<td></td>
</tr>
<tr>
<td>080H</td>
<td>P0</td>
<td>0/8</td>
<td></td>
</tr>
</tbody>
</table>

**Bit Addressable**

**Non Bit Addressable**
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>MSB</th>
<th>Bit Address and Symbol</th>
<th>LSB</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0</td>
<td>Port 0</td>
<td>80H</td>
<td>P0.7</td>
<td>P0.6</td>
<td>P0.5</td>
<td>P0.4</td>
</tr>
<tr>
<td>SP</td>
<td>Stack Pointer</td>
<td>81H</td>
<td></td>
<td></td>
<td></td>
<td>0000 0111B</td>
</tr>
<tr>
<td>DPTR</td>
<td>Data Pointer Low</td>
<td>82H</td>
<td></td>
<td></td>
<td></td>
<td>0000 0000B</td>
</tr>
<tr>
<td></td>
<td>Data Pointer High</td>
<td>83H</td>
<td></td>
<td></td>
<td></td>
<td>0000 0000B</td>
</tr>
<tr>
<td>PCON</td>
<td>Power Control</td>
<td>87H</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
</tr>
<tr>
<td>TCON</td>
<td>Timer Control</td>
<td>88H</td>
<td>TF1</td>
<td>TR1</td>
<td>TR0</td>
<td>IE1</td>
</tr>
<tr>
<td>TMOD</td>
<td>Timer Mode</td>
<td>89H</td>
<td>GATE</td>
<td>C/T</td>
<td>M1</td>
<td>M0</td>
</tr>
<tr>
<td>TL0</td>
<td>Timer Low 0</td>
<td>8AH</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TL1</td>
<td>Timer Low 1</td>
<td>8BH</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TH0</td>
<td>Timer High 0</td>
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<td></td>
<td></td>
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<tr>
<td>TH1</td>
<td>Timer High 1</td>
<td>8DH</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AUXR</td>
<td>Auxiliary register</td>
<td>8EH</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
</tr>
<tr>
<td>WAKE_CLKO</td>
<td>CLK Output</td>
<td>8EH</td>
<td>PCWAKEUP</td>
<td>AXD_PIN_B</td>
<td>T1_PIN_B</td>
<td>T0_PIN_B</td>
</tr>
<tr>
<td>P1</td>
<td>Port 1</td>
<td>90H</td>
<td>P1.7</td>
<td>P1.6</td>
<td>P1.5</td>
<td>P1.4</td>
</tr>
<tr>
<td>P1M1</td>
<td>P1 configuration 1</td>
<td>91H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P1M0</td>
<td>P1 configuration 0</td>
<td>92H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P0M1</td>
<td>P0 configuration 1</td>
<td>93H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P0M0</td>
<td>P0 configuration 0</td>
<td>94H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2M1</td>
<td>P2 configuration 1</td>
<td>95H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2M0</td>
<td>P2 configuration 0</td>
<td>96H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_DIV</td>
<td>Clock Divider</td>
<td>97H</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SCON</td>
<td>Serial Control</td>
<td>98H</td>
<td>SM0/FE</td>
<td>SM1</td>
<td>SM2</td>
<td>REN</td>
</tr>
<tr>
<td>SBUF</td>
<td>Serial Buffer</td>
<td>99H</td>
<td></td>
<td></td>
<td></td>
<td>xxx xxxxB</td>
</tr>
<tr>
<td>S2CON</td>
<td>S2 Control</td>
<td>9AH</td>
<td>S2SM0</td>
<td>S2SM1</td>
<td>S2SM2</td>
<td>S2REN</td>
</tr>
<tr>
<td>S2SBUF</td>
<td>S2 Serial Buffer</td>
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<td>xxx xxxxB</td>
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<td></td>
</tr>
<tr>
<td>BRT</td>
<td>dedicated Baud-Rate Timer</td>
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<td></td>
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</tr>
<tr>
<td>P1ASF</td>
<td>P1 Analog Special Function</td>
<td>9DH</td>
<td>P17ASF</td>
<td>P16ASF</td>
<td>P15ASF</td>
<td>P14ASF</td>
</tr>
<tr>
<td>P2</td>
<td>Port 2</td>
<td>A0H</td>
<td>P2.7</td>
<td>P2.6</td>
<td>P2.5</td>
<td>P2.4</td>
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<td>BUS_SPEED</td>
<td>Bus-Speed Control</td>
<td>A1H</td>
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<td>-</td>
<td>ALES1</td>
<td>ALES0</td>
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<tr>
<td>AUXR1</td>
<td>Auxiliary register1</td>
<td>A2H</td>
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<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
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<tr>
<td>IE</td>
<td>Interrupt Enable</td>
<td>A8H</td>
<td>EA</td>
<td>ELVD</td>
<td>EADC</td>
<td>ES</td>
</tr>
<tr>
<td>SADDR</td>
<td>Slave Address</td>
<td>A9H</td>
<td></td>
<td></td>
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<td>xxx xxxxB</td>
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<tr>
<td>IE2</td>
<td>Interrupt Enable 2</td>
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<td>-</td>
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<tr>
<td>P3</td>
<td>Port 3</td>
<td>B0H</td>
<td>P3.7</td>
<td>P3.6</td>
<td>P3.5</td>
<td>P3.4</td>
</tr>
<tr>
<td>P3M1</td>
<td>P2 configuration 1</td>
<td>B1H</td>
<td>0000 0000B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Address</td>
<td>Bit Address and Symbol</td>
<td>Value after Power-on or Reset</td>
<td></td>
<td></td>
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<td>P3 configuration 0</td>
<td>B2H</td>
<td>MSB</td>
<td>PS1</td>
<td>PS2</td>
<td>0000 0000B</td>
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<td>P4 configuration 1</td>
<td>B3H</td>
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<td>0000 0000B</td>
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<tr>
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<td>P4 configuration 0</td>
<td>B4H</td>
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<td></td>
<td></td>
<td>0000 0000B</td>
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<tr>
<td>IP2</td>
<td>2nd Interrupt Priority Low register</td>
<td>B5H</td>
<td></td>
<td></td>
<td></td>
<td>xxxxx xx00B</td>
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<tr>
<td>IP2H</td>
<td>2nd Interrupt Priority Low register</td>
<td>B6H</td>
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<td>xxxxx xx00B</td>
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<tr>
<td>IPH</td>
<td>Interrupt Priority High</td>
<td>B7H</td>
<td>PPCAH</td>
<td>PLVDH</td>
<td>PADCH</td>
<td>PSH</td>
</tr>
<tr>
<td>IP</td>
<td>Interrupt Priority Low</td>
<td>B8H</td>
<td>PPCA</td>
<td>PLVD</td>
<td>PADC</td>
<td>PS</td>
</tr>
<tr>
<td>SADEN</td>
<td>Slave Address Mask</td>
<td>B9H</td>
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<td></td>
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<tr>
<td>P4SW</td>
<td>Port 4 switch</td>
<td>BBH</td>
<td>LVD_P4.6</td>
<td>ALE_P4.5</td>
<td>NA_P4.4</td>
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<tr>
<td>ADC_CONTR</td>
<td>ADC Control</td>
<td>BCH</td>
<td>ADC_POWER</td>
<td>SPEED1</td>
<td>SPEED0</td>
<td>ADC_FLAG</td>
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<tr>
<td>ADC_RES</td>
<td>ADC Result</td>
<td>BDH</td>
<td></td>
<td></td>
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<tr>
<td>ADC_RESL</td>
<td>ADC Result Low</td>
<td>BEH</td>
<td></td>
<td></td>
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<tr>
<td>P4</td>
<td>Port 4</td>
<td>C0H</td>
<td>P4.7</td>
<td>P4.6</td>
<td>P4.5</td>
<td>P4.4</td>
</tr>
<tr>
<td>WDT_CONTR</td>
<td>Watch-Dog-Timer Control Register</td>
<td>C1H</td>
<td>WDT_FLAG</td>
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<td>EN_WDT</td>
<td>CLR_WDT</td>
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<tr>
<td>IAP_DATA</td>
<td>ISP/IAP Flash Data Register</td>
<td>C2H</td>
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<tr>
<td>IAP_ADDRH</td>
<td>ISP/IAP Flash Address High</td>
<td>C3H</td>
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<tr>
<td>IAP_ADDRL</td>
<td>ISP/IAP Flash Address Low</td>
<td>C4H</td>
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<td>IAP_CMD</td>
<td>ISP/IAP Flash Command Register</td>
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<td>-</td>
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<tr>
<td>IAP_TRIG</td>
<td>ISP/IAP Flash Command Trigger</td>
<td>C6H</td>
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<tr>
<td>IAP_CONTR</td>
<td>ISP/IAP Control Register</td>
<td>C7H</td>
<td>IAPEN</td>
<td>SWBS</td>
<td>SWRST</td>
<td>CMD_FAIL</td>
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<tr>
<td>P5</td>
<td>Port 5</td>
<td>C8H</td>
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<tr>
<td>P5M1</td>
<td>P5 Configuration 1</td>
<td>C9H</td>
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<tr>
<td>P5M0</td>
<td>P5 Configuration 0</td>
<td>CAH</td>
<td></td>
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<td></td>
<td></td>
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<tr>
<td>SPSTAT</td>
<td>SPI Status register</td>
<td>CDH</td>
<td>SPIF</td>
<td>WCOL</td>
<td>-</td>
<td>-</td>
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<tr>
<td>SPCTL</td>
<td>SPI control register</td>
<td>CEH</td>
<td>SSIG</td>
<td>SPEN</td>
<td>DORD</td>
<td>MSTR</td>
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<tr>
<td>SPDAT</td>
<td>SPI Data register</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td>PSW</td>
<td>Program Status Word</td>
<td>D0H</td>
<td>CY</td>
<td>AC</td>
<td>F0</td>
<td>RS1</td>
</tr>
<tr>
<td>CCON</td>
<td>PCA Control Register</td>
<td>D8H</td>
<td>CF</td>
<td>CR</td>
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<td>-</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Address</td>
<td>Bit Address and Symbol</td>
<td>Value after Power-on or Reset</td>
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<td></td>
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<td></td>
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<tr>
<td>CMOD</td>
<td>PCA Mode Register</td>
<td>D9H</td>
<td>CIDL - - - - CPS2 CPS1 CPS0 ECF</td>
<td>00xx 0000B</td>
<td></td>
<td></td>
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<tr>
<td>CCAPM0</td>
<td>PCA Module 0 Mode Register</td>
<td>DAH</td>
<td>- ECOM0 CAPP0 CAPN0 MAT0 TOG0 PWM0 ECCF0</td>
<td>x000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCAPM1</td>
<td>PCA Module 1 Mode Register</td>
<td>DBH</td>
<td>- ECOM1 CAPP1 CAPN1 MAT1 TOG1 PWM1 ECCF1</td>
<td>x000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ACC</td>
<td>Accumulator</td>
<td>E0H</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CL</td>
<td>PCA Base Timer Low</td>
<td>E9H</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCAP0L</td>
<td>PCA module 0 capture register low</td>
<td>EAH</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCAP1L</td>
<td>PCA module 1 capture register low</td>
<td>EBH</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>B Register</td>
<td>F0H</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCA_PWM0</td>
<td>PCA PWM mode auxiliary register 1</td>
<td>F2H</td>
<td>- - - - - - EPC0H EPC0L</td>
<td>xxxx xx00B</td>
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<td></td>
</tr>
<tr>
<td>PCA_PWM1</td>
<td>PCA PWM mode auxiliary register 1</td>
<td>F3H</td>
<td>- - - - - - EPC1H EPC1L</td>
<td>xxxx xx00B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CH</td>
<td>PCA Base Timer High</td>
<td>F9H</td>
<td></td>
<td>0000 0000B</td>
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<td></td>
</tr>
<tr>
<td>CCAP0H</td>
<td>PCA module 0 capture register high</td>
<td>FAH</td>
<td></td>
<td>0000 0000B</td>
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<td></td>
</tr>
<tr>
<td>CCAP1H</td>
<td>PCA module 1 capture register high</td>
<td>FBH</td>
<td></td>
<td>0000 0000B</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Accumulator**

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

**B-Register**

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

**Stack Pointer**

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.
Program Status Word (PSW)

The program status word (PSW) contains several status bits that reflect the current state of the CPU. The PSW, shown below, resides in the SFR space. It contains the Carry bit, the Auxiliary Carry (for BCD operation), the two register bank select bits, the Overflow flag, a Parity bit and two user-definable status flags.

The Carry bit, other than serving the function of a Carry bit in arithmetic operations, also serves as the “Accumulator” for a number of Boolean operations.

The bits RS0 and RS1 are used to select one of the four register banks shown in the previous page. A number of instructions refer to these RAM locations as R0 through R7.

The Parity bit reflects the number of 1s in the Accumulator. P=1 if the Accumulator contains an odd number of 1s and otherwise P=0.

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CY</td>
<td>AC</td>
<td>F0</td>
<td>RS1</td>
<td>RS0</td>
<td>OV</td>
<td>F1</td>
<td>P</td>
</tr>
</tbody>
</table>

**Data Pointer**

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

For fast data movement, STC12C5A60S2 supports two data pointers. They share the same SFR address and are switched by the register bit – DSP/AUXR.0.

<table>
<thead>
<tr>
<th>AUXR1 register</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit</td>
<td>B7</td>
</tr>
<tr>
<td>name</td>
<td>-</td>
</tr>
</tbody>
</table>

**PCA_P4**

0 : Default.
1 : The PCA function in P1 [4:2] is switched to P4[3:1].

**SPI_P4**

0 : Default.
1 : The SPI function in P1[7:4] is redirected to P4[3:0].
The following program is an assembly program that demonstrates how the dual data pointer be used.

```
AUXR1 DATA 0A2H ;Define special function register AUXR1
MOV AUXR1, #0 ;DPS=0, select DPTR0

MOV DPTR, #1FFH ;Set DPTR0 for 1FFH
MOV A, #55H
MOVX @DPTR, A ;load the value 55H in the 1FFH unit

MOV DPTR, #2FFH ;Set DPTR0 for 2FFH
MOV A, #0AAH
MOVX @DPTR, A ;load the value 0AAH in the 2FFH unit

INC AUXR1 ;DPS=1, DPTR1 is selected
MOV DPTR, #1FFH ;Set DPTR1 for 1FFH
MOVX A, @DPTR ;Get the content of 1FFH unit
;which is pointed by DPTR1,
;the content of Accumulator has changed for 55H

INC AUXR1 ;DPS=0, DPTR0 is selected
MOVX A, @DPTR ;Get the content of 2FFH unit
;which is pointed by DPTR0,
;the content of Accumulator has changed for 0AAH

INC AUXR1 ;DPS=1, DPTR1 is selected
MOVX A, @DPTR ;Get the content of 1FFH unit
;which is pointed by DPTR1,
;the content of Accumulator has changed for 55H

INC AUXR1 ;DPS=0, DPTR0 is selected
MOVX A, @DPTR ;Get the content of 2FFH unit
;which is pointed by DPTR0,
;the content of Accumulator has changed for 0AAH
```

S2_P4
0 : Default.
1 : The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].

GF2 : General Flag. It can be used by software.

ADRJ
0 : The 10-bit conversion result of ADC is arranged as {ADC_RES[7:0], ADC_RES[1:0]}.
1 : The 10-bit conversion result is right-justified, {ADC_RES[1:0], ADC_RES[7:0]}.

DPS
0 : Default.
1 : The secondary DPTR is switched to use.
5.2 Addressing Modes

Addressing modes are an integral part of each computer's instruction set. They allow specifying the source or destination of data in different ways, depending on the programming situation. There are eight modes available:

- Register
- Direct
- Indirect
- Immediate
- Relative
- Absolute
- Long
- Indexed

Direct Addressing (DIR)
In direct addressing, the operand is specified by an 8-bit address field in the instruction. Only internal data RAM and SFRs can be directly addressed.

Indirect Addressing (IND)
In indirect addressing, the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit data pointer register – DPTR.

Register Instruction (REG)
The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient because this mode eliminates the need of an extra address byte. When such instruction is executed, one of the eight registers in the selected bank is accessed.

Register-Specific Instruction
Some instructions are specific to a certain register. For example, some instructions always operate on the accumulator or data pointer, etc. No address byte is needed for such instructions. The opcode itself does it.

Immediate Constant (IMM)
The value of a constant can follow the opcode in the program memory.

Index Addressing
Only program memory can be accessed with indexed addressing and it can only be read. This addressing mode is intended for reading look-up tables in program memory. A 16-bit base register (either DPTR or PC) points to the base of the table, and the accumulator is set up with the table entry number. Another type of indexed addressing is used in the conditional jump instruction.

In conditional jump, the destination address is computed as the sum of the base pointer and the accumulator.
## 5.3 Instruction Set Summary

The STC MCU instructions are fully compatible with the standard 8051’s, which are divided among five functional groups:
- Arithmetic
- Logical
- Data transfer
- Boolean variable
- Program branching

The following tables provides a quick reference chart showing all the 8051 instructions. Once you are familiar with the instruction set, this chart should prove a handy and quick source of reference.

<table>
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<tr>
<th>Mnemonic</th>
<th>Description</th>
<th>Byte</th>
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<th>Execution clocks of STC12C5A60S2</th>
</tr>
</thead>
<tbody>
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<td>ADD A, Rn</td>
<td>Add register to Accumulator</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ADD A, direct</td>
<td>Add direct byte to Accumulator</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ADD A, @Ri</td>
<td>Add indirect RAM to Accumulator</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ADD A, #data</td>
<td>Add immediate data to Accumulator</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ADDC A, Rn</td>
<td>Add register to Accumulator with Carry</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ADDC A, direct</td>
<td>Add direct byte to Accumulator with Carry</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ADDC A, @Ri</td>
<td>Add indirect RAM to Accumulator with Carry</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ADDC A, #data</td>
<td>Add immediate data to Accumulator with Carry</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>SUBB A, Rn</td>
<td>Subtract Register from Accumulator with borrow</td>
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<td>12</td>
<td>2</td>
</tr>
<tr>
<td>SUBB A, direct</td>
<td>Subtract direct byte from Accumulator with borrow</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>SUBB A, @Ri</td>
<td>Subtract indirect RAM from Accumulator with borrow</td>
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<td>12</td>
<td>3</td>
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<tr>
<td>SUBB A, #data</td>
<td>Subtract immediate data from Accumulator with borrow</td>
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<td>12</td>
<td>2</td>
</tr>
<tr>
<td>INC A</td>
<td>Increment Accumulator</td>
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<td>2</td>
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<tr>
<td>INC Rn</td>
<td>Increment register</td>
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<td>3</td>
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<tr>
<td>INC direct</td>
<td>Increment direct byte</td>
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<td>12</td>
<td>4</td>
</tr>
<tr>
<td>INC @Ri</td>
<td>Increment direct RAM</td>
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<td>4</td>
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<td>DEC A</td>
<td>Decrement Accumulator</td>
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<td>DEC Rn</td>
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</tr>
<tr>
<td>DEC direct</td>
<td>Decrement direct byte</td>
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<td>12</td>
<td>4</td>
</tr>
<tr>
<td>DEC @Ri</td>
<td>Decrement indirect RAM</td>
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<td>4</td>
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<tr>
<td>INC DPTR</td>
<td>Increment Data Pointer</td>
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<td>MUL AB</td>
<td>Multiply A &amp; B</td>
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<td>48</td>
<td>4</td>
</tr>
<tr>
<td>DIV AB</td>
<td>Divide A by B</td>
<td>1</td>
<td>48</td>
<td>5</td>
</tr>
<tr>
<td>DA A</td>
<td>Decimal Adjust Accumulator</td>
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<td>12</td>
<td>4</td>
</tr>
<tr>
<td>Mnemonic</td>
<td>Description</td>
<td>Byte</td>
<td>Execution clocks of conventional 8051</td>
<td>Execution clocks of STC12C5A60S2</td>
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<tr>
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<td>----------------------------------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>ANL</td>
<td>A, Rn AND Register to Accumulator</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ANL</td>
<td>A, direct AND direct byte to Accumulator</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ANL</td>
<td>A, @Ri AND indirect RAM to Accumulator</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ANL</td>
<td>A, #data AND immediate data to Accumulator</td>
<td>2</td>
<td>12</td>
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</tr>
<tr>
<td>ANL</td>
<td>direct, A AND Accumulator to direct byte</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>ANL</td>
<td>direct,#data AND immediate data to direct byte</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>ORL</td>
<td>A, Rn OR register to Accumulator</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ORL</td>
<td>A, direct OR direct byte to Accumulator</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ORL</td>
<td>A, @Ri OR indirect RAM to Accumulator</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>ORL</td>
<td>A, #data OR immediate data to Accumulator</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>ORL</td>
<td>direct, A OR Accumulator to direct byte</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>ORL</td>
<td>direct,#data OR immediate data to direct byte</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>XRL</td>
<td>A, Rn Exclusive-OR register to Accumulator</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>XRL</td>
<td>A, direct Exclusive-OR direct byte to Accumulator</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>XRL</td>
<td>A, @Ri Exclusive-OR indirect RAM to Accumulator</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>XRL</td>
<td>A, #data Exclusive-OR immediate data to Accumulator</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>XRL</td>
<td>direct, A Exclusive-OR Accumulator to direct byte</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>XRL</td>
<td>direct,#data Exclusive-OR immediate data to direct byte</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>CLR</td>
<td>A Clear Accumulator</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>CPL</td>
<td>A Complement Accumulator</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>RL</td>
<td>A Rotate Accumulator Left</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>RLC</td>
<td>A Rotate Accumulator Left through the Carry</td>
<td>1</td>
<td>12</td>
<td>1</td>
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<tr>
<td>RR</td>
<td>A Rotate Accumulator Right</td>
<td>1</td>
<td>12</td>
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<tr>
<td>RRC</td>
<td>A Rotate Accumulator Right through the Carry</td>
<td>1</td>
<td>12</td>
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<tr>
<td>SWAP</td>
<td>A Swap nibbles within the Accumulator</td>
<td>1</td>
<td>12</td>
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<tr>
<td>Mnemonic</td>
<td>Description</td>
<td>Byte</td>
<td>Execution clocks of conventional 8051</td>
<td>Execution clocks of STC12C5A60S2</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------------------------------------</td>
<td>------</td>
<td>----------------------------------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>DATA TRANSFER</td>
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<td></td>
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<tr>
<td>MOV A, Rn</td>
<td>Move register to Accumulator</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>MOV A, direct</td>
<td>Move direct byte to Accumulator</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>MOV A, @Ri</td>
<td>Move indirect RAM to</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>MOV A, #data</td>
<td>Move immediate data to Accumulator</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>MOV Rn, A</td>
<td>Move Accumulator to register</td>
<td>1</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>MOV Rn, direct</td>
<td>Move direct byte to register</td>
<td>2</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>MOV Rn, #data</td>
<td>Move immediate data to register</td>
<td>2</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td>MOV direct, A</td>
<td>Move Accumulator to direct byte</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>MOV direct, Rn</td>
<td>Move register to direct byte</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>MOV direct, direct</td>
<td>Move direct byte to direct</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>MOV direct, @Ri</td>
<td>Move indirect RAM to direct byte</td>
<td>2</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>MOV direct, #data</td>
<td>Move immediate data to direct byte</td>
<td>3</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>MOV @Ri, A</td>
<td>Move Accumulator to indirect RAM</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>MOV @Ri, direct</td>
<td>Move direct byte to indirect RAM</td>
<td>2</td>
<td>24</td>
<td>4</td>
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<tr>
<td>MOV @Ri, #data</td>
<td>Move immediate data to indirect RAM</td>
<td>2</td>
<td>12</td>
<td>3</td>
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<tr>
<td>MOV DPTR, #data16</td>
<td>Move immediate data to indirect RAM</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>MOVC A,(@A+DPTR)</td>
<td>Move Code byte relative to DPTR to Acc</td>
<td>1</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>MOVC A, (@A+PC)</td>
<td>Move Code byte relative to PC to Acc</td>
<td>1</td>
<td>24</td>
<td>4</td>
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<tr>
<td>MOVX A, @Ri</td>
<td>Move External RAM(16-bit addr) to Acc</td>
<td>1</td>
<td>24</td>
<td>3</td>
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<tr>
<td>MOVX @Ri, A</td>
<td>Move Acc to External RAM(8-bit addr)</td>
<td>1</td>
<td>24</td>
<td>4</td>
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<tr>
<td>MOVX A, (@DPTR)</td>
<td>Move External RAM(16-bit addr) to Acc</td>
<td>1</td>
<td>24</td>
<td>3</td>
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<tr>
<td>MOVX @DPTR, A</td>
<td>Move Acc to External RAM(16-bit addr)</td>
<td>1</td>
<td>24</td>
<td>3</td>
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<tr>
<td>PUSH direct</td>
<td>Push direct byte onto stack</td>
<td>2</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>POP direct</td>
<td>POP direct byte from stack</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>XCH A, Rn</td>
<td>Exchange register with Accumulator</td>
<td>1</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>XCH A, direct</td>
<td>Exchange direct byte with Accumulator</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>XCH A, @Ri</td>
<td>Exchange indirect RAM with Accumulator</td>
<td>1</td>
<td>12</td>
<td>4</td>
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<tr>
<td>XCHD A, @Ri</td>
<td>Exchange low-order Digit indirect RAM with Acc</td>
<td>1</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>Mnemonic</td>
<td>Description</td>
<td>Byte</td>
<td>Execution clocks of conventional 8051</td>
<td>Execution clocks of STC12C5A60S2</td>
</tr>
<tr>
<td>----------</td>
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<tr>
<td><strong>BOOLEAN VARIABLE MANIPULATION</strong></td>
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<tr>
<td>CLR C</td>
<td>Clear Carry</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>CLR bit</td>
<td>Clear direct bit</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>SETB C</td>
<td>Set Carry</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>SETB bit</td>
<td>Set direct bit</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>CPL C</td>
<td>Complement Carry</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>CPL bit</td>
<td>Complement direct bit</td>
<td>2</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>ANL C, bit</td>
<td>AND direct bit to Carry</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>ANL C, /bit</td>
<td>AND complement of direct bit to Carry</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>ORL C, bit</td>
<td>OR direct bit to Carry</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>ORL C, /bit</td>
<td>OR complement of direct bit to Carry</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>MOV C, bit</td>
<td>Move direct bit to Carry</td>
<td>2</td>
<td>12</td>
<td>3</td>
</tr>
<tr>
<td>MOV bit, C</td>
<td>Move Carry to direct bit</td>
<td>2</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>JC rel</td>
<td>Jump if Carry is set</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>JNC rel</td>
<td>Jump if Carry not set</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>JB bit, rel</td>
<td>Jump if direct bit is set</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>JNB bit, rel</td>
<td>Jump if direct bit is not set</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>JBC bit, rel</td>
<td>Jump if direct bit is set &amp; clear bit</td>
<td>3</td>
<td>24</td>
<td>5</td>
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<tr>
<td><strong>PROGRAM BRANCHING</strong></td>
<td></td>
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<tr>
<td>ACALL addr11</td>
<td>Absolute Subroutine Call</td>
<td>2</td>
<td>24</td>
<td>6</td>
</tr>
<tr>
<td>LCALL addr16</td>
<td>Long Subroutine Call</td>
<td>3</td>
<td>24</td>
<td>6</td>
</tr>
<tr>
<td>RET</td>
<td>Return from Subroutine</td>
<td>1</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>RETI</td>
<td>Return from interrupt</td>
<td>1</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>AJMP addr11</td>
<td>Absolute Jump</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>LJMP addr16</td>
<td>Long Jump</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>SJMP rel</td>
<td>Short Jump (relative addr)</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>JMP @A+DPTR</td>
<td>Jump indirect relative to the DPTR</td>
<td>1</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>JZ rel</td>
<td>Jump if Accumulator is Zero</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>JNZ rel</td>
<td>Jump if Accumulator is not Zero</td>
<td>2</td>
<td>24</td>
<td>3</td>
</tr>
<tr>
<td>CJNE A, direct, rel</td>
<td>Compare direct byte to Acc and jump if not equal</td>
<td>3</td>
<td>24</td>
<td>5</td>
</tr>
<tr>
<td>CJNE A, #data, rel</td>
<td>Compare immediate to Acc and Jump if not equal</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>CJNE Rn, #data, rel</td>
<td>Compare immediate to register and Jump if not equal</td>
<td>3</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>CJNE @Ri, #data, rel</td>
<td>Compare immediate to indirect and jump if not equal</td>
<td>3</td>
<td>24</td>
<td>5</td>
</tr>
<tr>
<td>DJNZ Rn, rel</td>
<td>Decrement register and jump if not Zero</td>
<td>2</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>DJNZ direct, rel</td>
<td>Decrement direct byte and Jump if not Zero</td>
<td>3</td>
<td>24</td>
<td>5</td>
</tr>
<tr>
<td>NOP</td>
<td>No Operation</td>
<td>1</td>
<td>12</td>
<td>1</td>
</tr>
</tbody>
</table>
Instruction execution speed boost summary:
24 times faster execution speed 1
12 times faster execution speed 12
9.6 times faster execution speed 1
8 times faster execution speed 20
6 times faster execution speed 39
4.8 times faster execution speed 4
4 times faster execution speed 20
3 times faster execution speed 14
24 times faster execution speed 1

Based on the analysis of frequency of use order statistics, STC 1T series MCU instruction execution speed is faster than the traditional 8051 MCU 8 ~ 12 times in the same working environment.

Instruction execution clock count:
1 clock instruction 12
2 clock instruction 20
3 clock instruction 38
4 clock instruction 34
5 clock instruction 5
6 clock instruction 2
5.4 Instruction Definitions

ACALL  addr 11

Function: Absolute Call

Description: ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2K block of the program memory as the first byte of the instruction following ACALL. No flags are affected.

Example: Initially SP equals 07H. The label “SUBRTN” is at program memory location 0345H. After executing the instruction,

ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain 25H and 01H, respectively, and the PC will contain 0345H.

Bytes: 2

Cycles: 2

Encoding: a10 a9 a8 1 0 0 1 0   a7 a6 a5 a4   a3 a2 a1 a0

Operation:

ACALL
(PC)←(PC)+ 2
(SP)←(SP) + 1
((SP))←(PC7:0)
(SP)←(SP) + 1
((SP))←(PC15:8)
(PC10:0)←page address

ADD  A,<src-byte>

Function: Add

Description: ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct register-indirect, or immediate.

Example: The Accumulator holds 0C3H(11000011B) and register 0 holds 0AAH (10101010B). The instruction,

ADD  A,R0

will leave 6DH (01101101B) in the Accumulator with the AC flag cleared and both the carry flag and OV set to 1.
ADD   A,Rn
    Bytes:  1
    Cycles: 1
    Encoding: 0 0 1 0 1 r r r
    Operation: ADD
                (A)←(A) + (Rn)

ADD   A,direct
    Bytes:  2
    Cycles: 1
    Encoding: 0 0 1 0 0 1 0 1
                direct address
    Operation: ADD
                (A)←(A) + (direct)

ADD   A,@Ri
    Bytes:  1
    Cycles: 1
    Encoding: 0 0 1 0 0 1 1 1
    Operation: ADD
                (A)←(A) + ((Ri))

ADD   A,#data
    Bytes:  2
    Cycles: 1
    Encoding: 0 0 1 0 0 1 0 0
                immediate data
    Operation: ADD
                (A)←(A) + #data

ADDC   A,<src-byte>
Function: Add with Carry
Description: ADDC simultaneously adds the byte variable indicated, the Carry flag and the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred. OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not out of bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands.
Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C3H(11000011B) and register 0 holds 0AAH (10101010B) with the Carry. The instruction,
ADDC A,R0
will leave 6EH (01101101B) in the Accumulator with the AC flag cleared and both the carry flag and OV set to 1.
ADDCA,Rn

Bytes: 1
Cycles: 1
Encoding: 0 0 1 1 1 r r r
Operation: ADDC
(A) → (A) + (C) + (Rn)

ADDCA,direct

Bytes: 2
Cycles: 1
Encoding: 0 0 1 1 0 1 0 1
direct address
Operation: ADDC
(A) → (A) + (C) + (direct)

ADDCA,Ri

Bytes: 1
Cycles: 1
Encoding: 0 0 1 1 0 1 1 i
Operation: ADDC
(A) → (A) + (C) + ((Ri))

ADDCA,#data

Bytes: 2
Cycles: 1
Encoding: 0 0 1 1 0 1 0 0
immediate data
Operation: ADDC
(A) → (A) + (C) + #data

AJMP addr 11

Function: Absolute Jump
Description: AJMP transfers program execution to the indicated address, which is formed at run-time by concatenating the high-order five bits of the PC (after incrementing the PC twice), opcode bits 7-5, and the second byte of the instruction. The destination must therefore be within the same 2K block of program memory as the first byte of the instruction following AJMP.

Example: The label “JMPADR” is at program memory location 0123H. The instruction, AJMP JMPADR
is at location 0345H and will load the PC with 0123H.

Bytes: 2
Cycles: 2
Encoding: a10 a9 a8 a7 a6 a5 a4 a3 a2 a1 a0
Operation: AJMP
(SCR) → (SCR) + 2
(SCR) ← page address
ANL <dest-byte>, <src-byte>

**Function:** Logical-AND for byte variables

**Description:** ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

**Note:** When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch not the input pins.

**Example:** If the Accumulator holds 0C3H(11000011B) and register 0 holds 55H (01010101B) then the instruction, ANL A,R0
will leave 41H (01000001B) in the Accumulator.

When the destination is a directly addressed byte, this instruction will clear combinations of bits in any RAM location or hardware register. The mask byte determining the pattern of bits to be cleared would either be a constant contained in the instruction or a value computed in the Accumulator at run-time. The instruction, ANL Pl, #01110011B
will clear bits 7, 3, and 2 of output port 1.

**ANL A,Rn**

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**
  
  | 0 | 1 | 0 | 1 | l | r | r | r |

  **Operation:** ANL (A)→(A) ∧ (Rn)

**ANL A,direct**

- **Bytes:** 2
- **Cycles:** 1
- **Encoding:**
  
  | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

  **Operation:** ANL (A)→(A) ∧ (direct)

**ANL A,@Ri**

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**
  
  | 0 | 1 | 0 | 1 | 0 | 1 | 1 | i |

  **Operation:** ANL (A)→(A) ∧ ((Ri))
**ANL**  
A,#data  

<table>
<thead>
<tr>
<th>Bytes: 2</th>
<th>Cycles: 1</th>
<th>Encoding:</th>
<th>Operation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 1 0 1 0 0</td>
<td></td>
<td>ANL (A) ← (A) ∧ #data</td>
<td></td>
</tr>
</tbody>
</table>

**ANL**  
direct,A  

<table>
<thead>
<tr>
<th>Bytes: 2</th>
<th>Cycles: 1</th>
<th>Encoding:</th>
<th>Operation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 1 0 0 1 0</td>
<td></td>
<td>ANL (direct) ← (direct) ∧ (A)</td>
<td></td>
</tr>
</tbody>
</table>

**ANL**  
direct,#data  

<table>
<thead>
<tr>
<th>Bytes: 3</th>
<th>Cycles: 2</th>
<th>Encoding:</th>
<th>Operation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 1 0 0 1 1</td>
<td></td>
<td>ANL (direct) ← (direct) ∧ #data</td>
<td></td>
</tr>
</tbody>
</table>

**ANL**  
C , <src-bit>  

<table>
<thead>
<tr>
<th>Function: Logical-AND for bit variables</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description: If the Boolean value of the source bit is a logical 0 then clear the carry flag; otherwise leave the carry flag in its current state. A slash (“/”) preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.</td>
</tr>
<tr>
<td>Example: Set the carry flag if, and only if, P1.0 = 1, ACC. 7 = 1, and OV = 0:</td>
</tr>
<tr>
<td>MOV  C, P1.0 ;LOAD CARRY WITH INPUT PIN STATE</td>
</tr>
<tr>
<td>ANL  C, ACC.7 ;AND CARRY WITH ACCUM. BIT.7</td>
</tr>
<tr>
<td>ANL  C, /OV ;AND WITH INVERSE OF OVERFLOW FLAG</td>
</tr>
</tbody>
</table>

**ANL**  
C,bit  

<table>
<thead>
<tr>
<th>Bytes: 2</th>
<th>Cycles: 2</th>
<th>Encoding:</th>
<th>Operation:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 0 0 0 0 1 0</td>
<td></td>
<td>ANL (C) ← (C) ∧ (bit)</td>
<td></td>
</tr>
</tbody>
</table>
ANL C, /bit

Bytes: 2

Cycles: 2

Encoding: 

<table>
<thead>
<tr>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
</tr>
</thead>
</table>

Operation: ADD

(C) ← (C) ∧ (bit)

CJNE <dest-byte>, <src-byte>, rel

Function: Compare and Jump if Not Equal

Description: CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of <src-byte>; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations: the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

Example: The Accumulator contains 34H. Register 7 contains 56H. The first instruction in the sequence

```
CJNE R7,#60H, NOT-EQ
```

sets the carry flag and branches to the instruction at label NOT-EQ. By testing the carry flag, this instruction determines whether R7 is greater or less than 60H.

If the data being presented to Port 1 is also 34H, then the instruction,

```
WAIT: CJNE A,P1,WAIT
```

clears the carry flag and continues with the next instruction in sequence, since the Accumulator does equal the data read from P1. (If some other value was being input on P1, the program will loop at this point until the P1 data changes to 34H.)

CJNE A,direct,rel

Bytes: 3

Cycles: 2

Encoding: 

<table>
<thead>
<tr>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
</table>

Operation: (PC) ← (PC) + 3

IF (A) < (direct) THEN

(PC) ← (PC) + relative offset

IF (A) < (direct) THEN

(C) ← 1

ELSE

(C) ← 0
CJNE A,#data,rel
Bytes: 3
Cycles: 2
Encoding: 1 0 1 1 | 0 1 0 1
Operation: (PC) ← (PC) + 3
IF (A) <> (data)
THEN
(PC) ← (PC) + relative offset
IF (A) < (data)
THEN
(C) ← 1
ELSE
(C) ← 0

CJNE Rn,#data,rel
Bytes: 3
Cycles: 2
Encoding: 1 0 1 1 | 1 r r r
Operation: (PC) ← (PC) + 3
IF (Rn) <> (data)
THEN
(PC) ← (PC) + relative offset
IF (Rn) < (data)
THEN
(C) ← 1
ELSE
(C) ← 0

CJNE @Ri,#data,rel
Bytes: 3
Cycles: 2
Encoding: 1 0 1 1 | 0 1 0 1 i
Operation: (PC) ← (PC) + 3
IF ((Ri)) <> (data)
THEN
(PC) ← (PC) + relative offset
IF ((Ri)) < (data)
THEN
(C) ← 1
ELSE
(C) ← 0
CLR A

**Function:** Clear Accumulator

**Description:** The Accumulator is cleared (all bits set to zero). No flags are affected.

**Example:** The Accumulator contains 5CH (01011100B). The instruction,
CLR A
will leave the Accumulator set to 00H (00000000B).

**Bytes:** 1
**Cycles:** 1
**Encoding:**

```
1 1 1 0 0 1 0 0
```

**Operation:** CLR
(A) ← 0

CLR bit

**Function:** Clear bit

**Description:** The indicated bit is cleared (reset to zero). No other flags are affected. CLR can operate on the carry flag or any directly addressable bit.

**Example:** Port 1 has previously been written with 5DH (01011101B). The instruction,
CLR P1.2
will leave the port set to 59H (01011001B).

CLR C

**Bytes:** 1
**Cycles:** 1
**Encoding:**

```
1 1 0 0 0 0 1 1
```

**Operation:** CLR
(C) ← 0

CLR bit

**Bytes:** 2
**Cycles:** 1
**Encoding:**

```
1 1 0 0 0 0 1 0
```

**Operation:** CLR
(bit) ← 0
### CPL A

**Function:** Complement Accumulator  
**Description:** Each bit of the Accumulator is logically complemented (one’s complement). Bits which previously contained a one are changed to a zero and vice-versa. No flags are affected.  
**Example:** The Accumulator contains 5CH(01011100B). The instruction,  

\[ \text{CPL A} \]

will leave the Accumulator set to 0A3H (101000011B).

- **Bytes:** 1  
- **Cycles:** 1  
- **Encoding:** 1 1 1 1 0 1 0 0  
- **Operation:**  
  \[ \text{CPL (A) \leftrightarrow (A)} \]

### CPL bit

**Function:** Complement bit  
**Description:** The bit variable specified is complemented. A bit which had been a one is changed to zero and vice-versa. No other flags are affected. CLR can operate on the carry or any directly addressable bit.  
**Note:** When this instruction is used to modify an output pin, the value used as the original data will be read from the output data latch, not the input pin.  
**Example:** Port 1 has previously been written with 5DH (01011101B). The instruction,  

\[ \text{CLR P1.1} \]
\[ \text{CLR P1.2} \]

will leave the port set to 59H (01011001B).

- **Bytes:** 1  
- **Cycles:** 1  
- **Encoding:** 1 0 1 1 0 0 1 1  
- **Operation:**  
  \[ \text{CPL (C) \leftrightarrow (C)} \]

### CPL C

- **Bytes:** 2  
- **Cycles:** 1  
- **Encoding:** 1 0 1 1 0 0 1 0  
- **Operation:**  
  \[ \text{CPL (bit) \leftrightarrow (bit)} \]
## DA A

### Function:
Decimal-adjust Accumulator for Addition

### Description:
DA A adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variables (each in packed-BCD format), producing two four-bit digits. Any ADD or ADDC instruction may have been used to perform the addition.

If Accumulator bits 3-0 are greater than nine (xxxx1010-xxxx1111), or if the AC flag is one, six is added to the Accumulator producing the proper BCD digit in the low-order nibble. This internal addition would set the carry flag if a carry-out of the low-order four-bit field propagated through all high-order bits, but it would not clear the carry flag otherwise.

If the carry flag is now set or if the four high-order bits now exceed nine (1010xxxx-111xxxx), these high-order bits are incremented by six, producing the proper BCD digit in the high-order nibble. Again, this would set the carry flag if there was a carry-out of the high-order bits, but wouldn’t clear the carry. The carry flag thus indicates if the sum of the original two BCD variables is greater than 100, allowing multiple precision decimal addition. OV is not affected.

All of this occurs during the one instruction cycle. Essentially, this instruction performs the decimal conversion by adding 00H, 06H, 60H, or 66H to the Accumulator, depending on initial Accumulator and PSW conditions.

Note: DA A cannot simply convert a hexadecimal number in the Accumulator to BCD notation, nor does DA A apply to decimal subtraction.

### Example:
The Accumulator holds the value 56H (01010110B) representing the packed BCD digits of the decimal number 56. Register 3 contains the value 67H (01100111B) representing the packed BCD digits of the decimal number 67. The carry flag is set. The instruction sequence.

```
ADDC    A,R3
DA          A
```

will first perform a standard twos-complement binary addition, resulting in the value 0BEH (10111110) in the Accumulator. The carry and auxiliary carry flags will be cleared.

The Decimal Adjust instruction will then alter the Accumulator to the value 24H (00101000B), indicating the packed BCD digits of the decimal number 24, the low-order two digits of the decimal sum of 56, 67, and the carry-in. The carry flag will be set by the Decimal Adjust instruction, indicating that a decimal overflow occurred. The true sum 56, 67, and 1 is 124.

BCD variables can be incremented or decremented by adding 01H or 99H. If the Accumulator initially holds 30H (representing the digits of 30 decimal), then the instruction sequence,

```
ADD      A,#99H
DA         A
```

will leave the carry set and 29H in the Accumulator, since 30 + 99 = 129. The low-order byte of the sum can be interpreted to mean 30 – 1 = 29.
DEC byte

Function: Decrement

Description: The variable indicated is decremented by 1. An original value of 00H will underflow to 0FFH. No flags are affected. Four operand addressing modes are allowed: accumulator, register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: Register 0 contains 7FH (01111111B). Internal RAM locations 7EH and 7FH contain 00H and 40H, respectively. The instruction sequence,

```
DEC @R0
DEC R0
DEC @R0
```

will leave register 0 set to 7EH and internal RAM locations 7EH and 7FH set to 0FFH and 3FH.

DEC A

Bytes: 1
Cycles: 1
Encoding: 0 0 0 1 0 1 0 0

Operation: DEC
(A) ← (A) - 1

DEC Rn

Bytes: 1
Cycles: 1
Encoding: 0 0 0 1 0 0 0 1

Operation: DEC
(Rn) ← (Rn) - 1
DEC direct
Bytes: 2
Cycles: 1
Encoding: 0 0 0 1 0 1 0 1
direct address
Operation: DEC
(direct) \rightarrow (\text{direct}) - 1

DEC @Ri
Bytes: 1
Cycles: 1
Encoding: 0 0 0 1 0 1 1 i
Operation: DEC
((\text{Ri})) \rightarrow ((\text{Ri})) - 1

DIV AB
Function: Divide
Description: DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B. The Accumulator receives the integer part of the quotient; register B receives the integer remainder. The carry and OV flags will be cleared.

Exception: if B had originally contained 00H, the values returned in the Accumulator and B-register will be undefined and the overflow flag will be set. The carry flag is cleared in any case.

Example: The Accumulator contains 251(OFBH or 11111011B) and B contains 18(12H or 00010010B). The instruction,

\[ \text{DIV AB} \]

will leave 13 in the Accumulator (0DH or 00001101B) and the value 17 (11H or 00010010B) in B, since 251 = (13 \times 18) + 17. Carry and OV will both be cleared.

Bytes: 1
Cycles: 4
Encoding: 1 0 0 0 0 1 0 0
Operation: DIV
\[
(A)_{15,8} \leftarrow (A)/(B)
\]
\[
(B)_{7,0} \leftarrow (A)/(B)
\]
DJNZ  <byte>, <rel-addr>

Function: Decrement and Jump if Not Zero
Description: DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H will underflow to 0FFH. No flags are affected. The branch destination would be computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction.

The location decremented may be a register or directly addressed byte.
Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: Internal RAM locations 40H, 50H, and 60H contain the values 01H, 70H, and 15H, respectively. The instruction sequence,

DJNZ  40H, LABEL_1
DJNZ  50H, LABEL_2
DJNZ  60H, LABEL_3

will cause a jump to the instruction at label LABEL_2 with the values 00H, 6FH, and 15H in the three RAM locations. The first jump was not taken because the result was zero.

This instruction provides a simple way of executing a program loop a given number of times, or for adding a moderate time delay (from 2 to 512 machine cycles) with a single instruction.

The instruction sequence,

MOV          R2,#8
TOOOLE:      CPL           P1.7
DJNZ          R2, TOOGLE

will toggle P1.7 eight times, causing four output pulses to appear at bit 7 of output Port 1. Each pulse will last three machine cycles; two for DJNZ and one to alter the pin.

DJNZ  Rn,rel

Bytes:  2
Cycles:  2
Encoding:  1 1 0 1  l  r  r  r  rel. address
Operation: DJNZ
(PC) ← (PC) + 2
(Rn) ← (Rn) – 1
IF (Rn) > 0 or (Rn) < 0
THEN
(PC) ← (PC)+ rel

DJNZ  direct, rel

Bytes:  3
Cycles:  2
Encoding:  1 1 0 1  0 1 0 1  direct address  rel. address
Operation: DJNZ
(\text{PC}) \leftarrow (\text{PC}) + 2
(direct) \leftarrow (\text{direct}) - 1
\text{IF} (\text{direct}) > 0 \text{ or } (\text{direct}) < 0
\text{THEN}
(\text{PC}) \leftarrow (\text{PC}) + \text{rel}

\text{INC} \ <\text{byte}>

Function: Increment
Description: \text{INC} \text{ increments the indicated variable by 1. An original value of 0FFH will overflow to 00H. No flags are affected. Three addressing modes are allowed: register, direct, or register-indirect.}

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: Register 0 contains 7EH (011111110B). Internal RAM locations 7EH and 7FH contain 0FFH and 40H, respectively. The instruction sequence,
\text{INC} \ @R0
\text{INC} \ R0
\text{INC} \ @R0

\text{will leave register 0 set to 7FH and internal RAM locations 7EH and 7FH holding (respectively) 00H and 41H.}

\text{INC} \ A
\begin{itemize}
  \item Bytes: 1
  \item Cycles: 1
  \item Encoding: \begin{array}{c|c|c|c}
    0 & 0 & 0 & 0 \\
    0 & 1 & 0 & 0
  \end{array}
  \item Operation: \text{INC} \\
  \text{(A)} \leftarrow (\text{A})+1
\end{itemize}

\text{INC} \ Rn
\begin{itemize}
  \item Bytes: 1
  \item Cycles: 1
  \item Encoding: \begin{array}{c|c|c|c|c}
    0 & 0 & 0 & 0 & 1 \end{array}
  \item Operation: \text{INC} \\
  (\text{Rn}) \leftarrow (\text{Rn})+1
\end{itemize}

\text{INC} \ \text{direct}
\begin{itemize}
  \item Bytes: 2
  \item Cycles: 1
  \item Encoding: \begin{array}{c|c|c|c|c|c}
    0 & 0 & 0 & 0 & 0 & 1 \\
    0 & 1 & 0 & 1 \end{array} \text{direct address}
  \item Operation: \text{INC} \\
  (\text{direct}) \leftarrow (\text{direct}) \text{+ 1}
\end{itemize}
INC  @Ri

Bytes: 1
Cycles: 1
Encoding: 0 0 0 0 0 1 1 i
Operation: INC
((Ri)) ← ((Ri)) + 1

INC  DPTR

Function: Increment Data Pointer
Description: Increment the 16-bit data pointer by 1. A 16-bit increment (modulo 2^16) is performed; an overflow of the low-order byte of the data pointer (DPL) from 0FFH to 00H will increment the high-order-byte (DPH). No flags are affected. This is the only 16-bit register which can be incremented.
Example: Register DPH and DPL contains 12H and 0FEH, respectively. The instruction sequence,
INC  DPTR
INC  DPTR
INC  DPTR
INC  DPTR
will change DPH and DPL to 13H and 01H.
Bytes: 1
Cycles: 2
Encoding: 1 0 1 0 0 0 1 1
Operation: INC
(DPTR) ← (DPTR) + 1

JB  bit, rel

Function: Jump if Bit set
Description: If the indicated bit is a one, jump to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. The bit tested is not modified. No flags are affected.
Example: The data present at input port 1 is 11001010B. The Accumulator holds 56 (01010110B). The instruction sequence,
JB  P1.2, LABEL1
JB  ACC.2, LABEL2
will cause program execution to branch to the instruction at label LABEL2.
Bytes: 3
Cycles: 2
Encoding: 0 0 1 0 0 0 0
Operation: JB
(PC) ← (PC) + 3
IF (bit) = 1
THEN
(PC) ← (PC) + rel
JBC  bit, rel

**Function:** Jump if Bit is set and Clear bit

**Description:** If the indicated bit is one, branch to the address indicated; otherwise proceed with the next instruction. The bit will not be cleared if it is already a zero. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. No flags are affected.

**Note:** When this instruction is used to test an output pin, the value used as the original data will be read from the output data latch, not the input pin.

**Example:** The Accumulator holds 56H (01010110B). The instruction sequence,

JBC  ACC.3, LABEL1
JBC  ACC.2, LABEL2

will cause program execution to continue at the instruction identified by the label LABEL2, with the Accumulator modified to 52H (01010010B).

**Bytes:** 3

**Cycles:** 2

**Encoding:**

<table>
<thead>
<tr>
<th>bit address</th>
<th>rel. address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 1</td>
<td>0 0 0 0</td>
</tr>
</tbody>
</table>

**Operation:**

JBC  
(PC) ← (PC) + 3
IF (bit) = 1
 THEN
   (bit) ← 0
   (PC) ← (PC) + rel

JC  rel

**Function:** Jump if Carry is set

**Description:** If the carry flag is set, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. No flags are affected.

**Example:** The carry flag is cleared. The instruction sequence,

JC  LABEL1
CPL  C
JC  LABEL2

will set the carry and cause program execution to continue at the instruction identified by the label LABEL2.

**Bytes:** 2

**Cycles:** 2

**Encoding:**

<table>
<thead>
<tr>
<th>rel. address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 0 0</td>
</tr>
</tbody>
</table>

**Operation:**

JC  
(PC) ← (PC) + 2
IF (C) = 1
 THEN
   (PC) ← (PC) + rel
JMP  @A+DPTR

Function: Jump indirect

Description: Add the eight-bit unsigned contents of the Accumulator with the sixteen-bit data pointer, and load the resulting sum to the program counter. This will be the address for subsequent instruction fetches. Sixteen-bit addition is performed (modulo $2^{16}$): a carry-out from the low-order eight bits propagates through the higher-order bits. Neither the Accumulator nor the Data Pointer is altered. No flags are affected.

Example: An even number from 0 to 6 is in the Accumulator. The following sequence of instructions will branch to one of four AJMP instructions in a jump table starting at JMP_TBL:

```
MOV DPTR, #JMP_TBL
JMP @A+DPTR
```

JMP_TBL:
AJMP LABEL0
AJMP LABEL1
AJMP LABEL2
AJMP LABEL3

If the Accumulator equals 04H when starting this sequence, execution will jump to label LABEL2. Remember that AJMP is a two-byte instruction, so the jump instructions start at every other address.

Bytes: 1
Cycles: 2
Encoding: 0 1 1 1 0 0 0 1 1

Operation:

```
(JP) \Rightarrow (A) + (DPTR)
```

JNB  bit, rel

Function: Jump if Bit is not set

Description: If the indicated bit is a zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. The bit tested is not modified. No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56H (01010110B). The instruction sequence,

```
JNB P1.3, LABEL1
JNB ACC.3, LABEL2
```

will cause program execution to continue at the instruction at label LABEL2

Bytes: 3
Cycles: 2
Encoding: 0 0 1 1 0 0 0 0

Operation:

```
(JP) \Rightarrow (JP) + 3
IF \ (bit) = 0
THEN \ (JP) \Rightarrow (JP) + \ rel
```
JNC rel

**Function:** Jump if Carry not set

**Description:** If the carry flag is a zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice to point to the next instruction. The carry flag is not modified.

**Example:** The carry flag is set. The instruction sequence,

```
JNC LABEL1
CPL C
JNC LABEL2
```

will clear the carry and cause program execution to continue at the instruction identified by the label LABEL2.

**Bytes:** 2

**Cycles:** 2

**Encoding:**

```
0 1 0 1 0 0 0 0
```

**Operation:**

```
JNC
(PC) ← (PC) + 2
IF (C) = 0
THEN (PC) ← (PC) + rel
```

JNZ rel

**Function:** Jump if Accumulator Not Zero

**Description:** If any bit of the Accumulator is a one, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

**Example:** The Accumulator originally holds 00H. The instruction sequence,

```
JNZ LABEL1
INC A
JNZ LABEL2
```

will set the Accumulator to 01H and continue at label LABEL2.

**Bytes:** 2

**Cycles:** 2

**Encoding:**

```
0 1 1 1 0 0 0 0
```

**Operation:**

```
JNZ
(PC) ← (PC) + 2
IF (A) ≠ 0
THEN (PC) ← (PC) + rel
```
### JZ rel

**Function:** Jump if Accumulator Zero

**Description:** If all bits of the Accumulator are zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

**Example:** The Accumulator originally contains 01H. The instruction sequence,

```
JZ   LABEL1
DEC   A
JZ   LAEEL2
```

will change the Accumulator to 00H and cause program execution to continue at the instruction identified by the label LABEL2.

**Bytes:** 2

**Cycles:** 2

**Encoding:**

```
0 1 1 0 0 0 0 0
```

**Operation:**

```
JZ
(PC) ← (PC) + 2
IF (A) = 0 THEN (PC) ← (PC) + rel
```

### LCALL addr16

**Function:** Long call

**Description:** LCALL calls a subroutine located at the indicated address. The instruction adds three to the program counter to generate the address of the next instruction and then pushes the 16-bit result onto the stack (low byte first), incrementing the Stack Pointer by two. The high-order and low-order bytes of the PC are then loaded, respectively, with the second and third bytes of the LCALL instruction. Program execution continues with the instruction at this address. The subroutine may therefore begin anywhere in the full 64K-byte program memory address space. No flags are affected.

**Example:** Initially the Stack Pointer equals 07H. The label “SUBRTN” is assigned to program memory location 1234H. After executing the instruction,

```
LCALL   SUBRTN
```

at location 0123H, the Stack Pointer will contain 09H, internal RAM locations 08H and 09H will contain 26H and 01H, and the PC will contain 1234H.

**Bytes:** 3

**Cycles:** 2

**Encoding:**

```
0 0 0 1 0 0 1 0
```

**Operation:**

```
LCALL
(PC) ← (PC) + 3
(SP) ← (SP) + 1
(((SP)) ← (PC) + rel)
(SP) ← (SP) + 1
(((SP)) ← (PC) + addr15-addr8
(PC) ← addr15-addr0
```
**LJMP addr16**

**Function:** Long Jump

**Description:** LJMP causes an unconditional branch to the indicated address, by loading the high-order and low-order bytes of the PC (respectively) with the second and third instruction bytes. The destination may therefore be anywhere in the full 64K program memory address space. No flags are affected.

**Example:** The label “JMPADR” is assigned to the instruction at program memory location 1234H. The instruction,

LJMP JMPADR

at location 0123H will load the program counter with 1234H.

**Bytes:** 3

**Cycles:** 2

**Encoding:**

<table>
<thead>
<tr>
<th></th>
<th>addr15-addr8</th>
<th>addr7-addr0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 0 0</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

**Operation:**

LJMP

(PC) ← addr15-addr8

**MOV <dest-byte> , <src-byte>**

**Function:** Move byte variable

**Description:** The byte variable indicated by the second operand is copied into the location specified by the first operand. The source byte is not affected. No other register or flag is affected.

This is by far the most flexible operation. Fifteen combinations of source and destination addressing modes are allowed.

**Example:** Internal RAM location 30H holds 40H. The value of RAM location 40H is 10H. The data present at input port 1 is 11001010B (0CAH).

MOV R0, #30H ;R0 < = 30H
MOV A, @R0 ;A < = 40H
MOV R1, A ;R1 < = 40H
MOV B, @R1 ;B < = 10H
MOV @R1, Pl ;RAM (40H) < = 0CAH
MOV P2, P1 ;P2 #0CAH

leaves the value 30H in register 0, 40H in both the Accumulator and register 1, 10H in register B, and 0CAH(11001010B) both in RAM location 40H and output on port 2.

**MOV A,Rn**

**Bytes:** 1

**Cycles:** 1

**Encoding:**

<table>
<thead>
<tr>
<th></th>
<th>r</th>
<th>r</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 1 1 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Operation:**

MOV

(A) ← (Rn)
*MOV A, direct
  Bytes: 2
  Cycles: 1
  Encoding: 1 1 1 0 0 1 0 1
  Operation: MOV (A) ← (direct)

*MOV A, ACC is not a valid instruction

MOV A, @Ri
  Bytes: 1
  Cycles: 1
  Encoding: 1 1 1 0 0 1 1 1
  Operation: MOV (A) ← ((Ri))

MOV A, #data
  Bytes: 2
  Cycles: 1
  Encoding: 0 1 1 1 0 1 0 0
  Operation: MOV (A) ← #data

MOV Rn, A
  Bytes: 1
  Cycles: 1
  Encoding: 1 1 1 1 1 r r r
  Operation: MOV (Rn) ← (A)

MOV Rn, direct
  Bytes: 2
  Cycles: 2
  Encoding: 1 0 1 0 1 r r r
  Operation: MOV (Rn) ← (direct)

MOV Rn, #data
  Bytes: 2
  Cycles: 1
  Encoding: 0 1 1 1 1 r r r
  Operation: MOV (Rn) ← #data
MOV direct, A
Bytes: 2
Cycles: 1
Encoding: 1111 0101
Operation: MOV (direct) ← (A)

MOV direct, Rn
Bytes: 2
Cycles: 2
Encoding: 1000 1rrr
Operation: MOV (direct) ← (Rn)

MOV direct, direct
Bytes: 3
Cycles: 2
Encoding: 1000 0101
Operation: MOV (direct) ← (direct)

MOV direct, @Ri
Bytes: 2
Cycles: 2
Encoding: 1000 0111
Operation: MOV (direct) ← (@Ri)

MOV direct,#data
Bytes: 3
Cycles: 2
Encoding: 0111 0101
Operation: MOV (direct) ← #data

MOV @Ri, A
Bytes: 1
Cycles: 1
Encoding: 1111 011i
Operation: MOV ((Ri)) ← (A)
MOV @Ri, direct

Bytes: 2
Cycles: 2
Encoding: 
Operation: MOV ((Ri)) ← (direct)

MOV @Ri, #data

Bytes: 2
Cycles: 1
Encoding: 
Operation: MOV ((Ri)) ← #data

MOV <dest-bit> , <src-bit>

Function: Move bit data
Description: The Boolean variable indicated by the second operand is copied into the location specified by the first operand. One of the operands must be the carry flag; the other may be any directly addressable bit. No other register or flag is affected.
Example: The carry flag is originally set. The data present at input Port 3 is 11000101B. The data previously written to output Port 1 is 35H (00110101B).

MOV P1.3, C
MOV C, P3.3
MOV P1.2, C

will leave the carry cleared and change Port 1 to 39H (00111001B).

MOV C,bit

Bytes: 2
Cycles: 1
Encoding: 
Operation: MOV (C) ← (bit)

MOV bit,C

Bytes: 2
Cycles: 2
Encoding: 
Operation: MOV (bit) ← (C)
MOV  DPTR, #data 16

Function: Load Data Pointer with a 16-bit constant
Description: The Data Pointer is loaded with the 16-bit constant indicated. The 16-bit constant is loaded into the second and third bytes of the instruction. The second byte (DPH) is the high-order byte, while the third byte (DPL) holds the low-order byte. No flags are affected. This is the only instruction which moves 16 bits of data at once.

Example: The instruction,
MOV  DPTR, #1234H
will load the value 1234H into the Data Pointer: DPH will hold 12H and DPL will hold 34H.

Bytes: 3
Cycles: 2
Encoding:

| 1   | 0   | 0   | 1   | 0   | 0   | 0   | 0   | immediate | data 15-8 |

Operation:

MOV  (DPTR) ← #data_{15,0}
DPH  DPL ← #data_{15,8} #data_{7,0}

MOVC  A, @A+ <base-reg>

Function: Move Code byte
Description: The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, the PC is incremented to the address of the following instruction before being added with the Accumulator; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example: A value between 0 and 3 is in the Accumulator. The following instructions will translate the value in the Accumulator to one of four values defined by the DB (define byte) directive.
REL-PC: INC  A
MOVC  A, @A+PC
RET
DB   66H
DB   77H
DB   88H
DB   99H

If the subroutine is called with the Accumulator equal to 01H, it will return with 77H in the Accumulator. The INC A before the MOVC instruction is needed to “get around” the RET instruction above the table. If several bytes of code separated the MOVC from the table, the corresponding number would be added to the Accumulator instead.

MOVC  A, @A+DPTR

Bytes: 1
Cycles: 2
Encoding:

| 1   | 0   | 0   | 1   | 0   | 1   | 1   |

Operation:

MOVC  (A) ← ((A)+(DPTR))
MOVC A, @A+PC

<table>
<thead>
<tr>
<th>Function</th>
<th>Move External</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description:</td>
<td>The MOVC instructions transfer data between the Accumulator and a byte of external data memory, hence the “X” appended to MOV. There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.</td>
</tr>
</tbody>
</table>

In the first type, the contents of R0 or R1 in the current register bank provide an eight-bit address multiplexed with data on P0. Eight bits are sufficient for external I/O expansion decoding or for a relatively small RAM array. For somewhat larger arrays, any output port pins can be used to output higher-order address bits. These pins would be controlled by an output instruction preceding the MOVC.

In the second type of MOVC instruction, the Data Pointer generates a sixteen-bit address. P2 outputs the high-order eight address bits (the contents of DPH) while P0 multiplexes the low-order eight bits (DPL) with data. The P2 Special Function Register retains its previous contents while the P2 output buffers are emitting the contents of DPH. This form is faster and more efficient when accessing very large data arrays (up to 64K bytes), since no additional instructions are needed to set up the output ports.

It is possible in some situations to mix the two MOVC types. A large RAM array with its high-order address lines driven by P2 can be addressed via the Data Pointer, or with code to output high-order address bits to P2 followed by a MOVC instruction using R0 or R1.

Example: An external 256 byte RAM using multiplexed address/data lines (e.g., an Intel 8155 RAM/I/O/Timer) is connected to the 8051 Port 0. Port 3 provides control lines for the external RAM. Ports 1 and 2 are used for normal I/O. Registers 0 and 1 contain 12H and 34H. Location 34H of the external RAM holds the value 56H. The instruction sequence,

```
MOVX A, @R1
MOVX @R0, A
```

copies the value 56H into both the Accumulator and external RAM location 12H.
MOVX  A, @DPTR  
Bytes: 1  
Cycles: 2  
Encoding: 1 1 1 0 0 0 0 0  
Operation: MOVX  
(A) ← ((DPTR))  

MOVX  @Ri, A  
Bytes: 1  
Cycles: 2  
Encoding: 1 1 1 1 0 0 1 i  
Operation: MOVX  
((Ri)) ← (A)  

MOVX  @DPTR, A  
Bytes: 1  
Cycles: 2  
Encoding: 1 1 1 1 0 0 0 0  
Operation: MOVX  
(DPTR) ← (A)  

MUL  AB  
Function: Multiply  
Description: MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (0FFH) the overflow flag is set; otherwise it is cleared. The carry flag is always cleared.  
Example: Originally the Accumulator holds the value 80 (50H). Register B holds the value 160 (0A0H). The instruction,  

   MUL  AB  

will give the product 12,800 (3200H), so B is changed to 32H (00110010B) and the Accumulator is cleared. The overflow flag is set, carry is cleared.  
Bytes: 1  
Cycles: 4  
Encoding: 1 0 1 0 0 1 0 0  
Operation: MUL  
(A)_{7:0} ← (A) × (B)  
(B)_{15:8}
NOP

Function: No Operation
Description: Execution continues at the following instruction. Other than the PC, no registers or flags are affected.
Example: It is desired to produce a low-going output pulse on bit 7 of Port 2 lasting exactly 5 cycles. A simple SETB/CLR sequence would generate a one-cycle pulse, so four additional cycles must be inserted. This may be done (assuming no interrupts are enabled) with the instruction sequence.

CLR            P2.7
NOP
NOP
NOP
NOP
SETB            P2.7

Bytes: 1
Cycles: 1
Encoding: 0 0 0 0 0 0 0 0
Operation: NOP
(PC) ← (PC)+1

ORL <dest-byte> , <src-byte>

Function: Logical-OR for byte variables
Description: ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte. No flags are affected.
The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and R0 holds 55H (01010101B) then the instruction,

ORL A, R0

will leave the Accumulator holding the value 0D7H (11010111B). When the destination is a directly addressed byte, the instruction can set combinations of bits in any RAM location or hardware register. The pattern of bits to be set is determined by a mask byte, which may be either a constant data value in the instruction or a variable computed in the Accumulator at run-time. The instruction,

ORL P1, #00110010B

will set bits 5, 4, and 1 of output Port 1.
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Bytes</th>
<th>Cycles</th>
<th>Encoding</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ORL A,Rn</strong></td>
<td>1</td>
<td>1</td>
<td>0 1 0 0 1 r r r</td>
<td>ORL (A \leftarrow (A) \lor (Rn))</td>
</tr>
<tr>
<td><strong>ORL A,direct</strong></td>
<td>2</td>
<td>1</td>
<td>0 1 0 0 0 1 0 1</td>
<td>direct address</td>
</tr>
<tr>
<td><strong>ORL A,@Ri</strong></td>
<td>1</td>
<td>1</td>
<td>0 1 0 0 0 1 1 i</td>
<td>ORL (A \leftarrow (A) \lor ((Ri)))</td>
</tr>
<tr>
<td><strong>ORL A,#data</strong></td>
<td>2</td>
<td>1</td>
<td>0 1 0 0 0 1 0 0</td>
<td>immediate data</td>
</tr>
<tr>
<td><strong>ORL direct, A</strong></td>
<td>2</td>
<td>1</td>
<td>0 1 0 0 0 0 1 0</td>
<td>direct address</td>
</tr>
<tr>
<td><strong>ORL direct, #data</strong></td>
<td>3</td>
<td>2</td>
<td>0 1 0 0 0 0 1 1</td>
<td>direct address immediate data</td>
</tr>
<tr>
<td><strong>ORL direct, A</strong></td>
<td>2</td>
<td>1</td>
<td>0 1 0 0 0 0 1 0</td>
<td>direct address</td>
</tr>
</tbody>
</table>
ORL  C, <src-bit>

Function: Logical-OR for bit variables

Description: Set the carry flag if the Boolean value is a logical 1; leave the carry in its current state otherwise. A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.

Example: Set the carry flag if and only if P1.0 = 1, ACC. 7 = 1, or OV = 0:
MOV    C, P1.0           ;LOAD CARRY WITH INPUT PIN P10
ORL    C, ACC.7          ;OR CARRY WITH THE ACC.BIT 7
ORL    C, /OV            ;OR CARRY WITH THE INVERSE OF OV

ORL  C, bit

Bytes: 2
Cycles: 2

Encoding: 0 1 1 1 0 0 1 0  

Operation: ORL (C) ← (C) ∨ (bit)

ORL  C, /bit

Bytes: 2
Cycles: 2

Encoding: 1 0 1 0 0 0 0 0  

Operation: ORL (C) ← (C) ∨ (bit)

POP  direct

Function: Pop from stack

Description: The contents of the internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

Example: The Stack Pointer originally contains the value 32H, and internal RAM locations 30H through 32H contain the values 20H, 23H, and 01H, respectively. The instruction sequence, 
POP    DPH
POP    DPL
will leave the Stack Pointer equal to the value 30H and the Data Pointer set to 0123H. At this point the instruction,
POP    SP
will leave the Stack Pointer set to 20H. Note that in this special case the Stack Pointer was decremented to 2FH before being loaded with the value popped (20H).

Bytes: 2
Cycles: 2

Encoding: 1 1 0 1 0 0 0 0  

Operation: POP (diect) ← ((SP))
(SP) ← (SP) - 1
PUSH    direct

Function:    Push onto stack
Description: The Stack Pointer is incremented by one. The contents of the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.
Example:    On entering interrupt routine the Stack Pointer contains 09H. The Data Pointer holds the value 0123H. The instruction sequence,

```
PUSH     DPL
PUSH     DPH
```

will leave the Stack Pointer set to 0BH and store 23H and 01H in internal RAM locations 0AH and 0BH, respectively.

Bytes:    2
Cycles:    2
Encoding: 1 1 0 0 0 0 0 0
direct address
Operation: PUSH
(SP) ← (SP) + 1
((SP)) ← (direct)

RET

Function:    Return from subroutine
Description: RET pops the high- and low-order bytes of the PC successively from the stack, decrementing the Stack Pointer by two. Program execution continues at the resulting address, generally the instruction immediately following an ACALL or LCALL. No flags are affected.
Example:    The Stack Pointer originally contains the value 0BH. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

```
RET
```

will leave the Stack Pointer equal to the value 09H. Program execution will continue at location 0123H.

Bytes:    1
Cycles:    2
Encoding: 0 0 1 0 0 0 1 0
Operation: RET
(“PC”_15:8) ← ((SP))
(SP) ← (SP) - 1
(“PC”_7:0) ← ((SP))
(SP) ← (SP) - 1
RETI

Function: Return from interrupt

Description: RETI pops the high- and low-order bytes of the PC successively from the stack, and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed. The Stack Pointer is left decremented by two. No other registers are affected; the PSW is not automatically restored to its pre-interrupt status. Program execution continues at the resulting address, which is generally the instruction immediately after the point at which the interrupt request was detected. If a lower- or same-level interrupt had been pending when the RETI instruction is executed, that one instruction will be executed before the pending interrupt is processed.

Example: The Stack Pointer originally contains the value 0BH. An interrupt was detected during the instruction ending at location 0122H. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

```
RETI
```

will leave the Stack Pointer equal to 09H and return program execution to location 0123H.

Bytes: 1

Cycles: 2

Encoding: 0 0 1 1 0 0 1 0

Operation:

```
RETI
(PC_{15:8}) \leftarrow ((SP))
(SP) \leftarrow (SP) -1
(PC_{7:0}) \leftarrow ((SP))
(SP) \leftarrow (SP) -1
```

RL A

Function: Rotate Accumulator Left

Description: The eight bits in the Accumulator are rotated one bit to the left. Bit 7 is rotated into the bit 0 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

```
RL A
```

leaves the Accumulator holding the value 8BH (10001011B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding: 0 0 1 0 0 0 1 1

Operation:

```
RL
(A_{n+1}) \leftarrow (A_n) \quad n = 0-6
(A_0) \leftarrow (A_7)
```
RLC A

**Function:**
Rotate Accumulator Left through the Carry flag

**Description:**
The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag; the original state of the carry flag moves into the bit 0 position. No other flags are affected.

**Example:**
The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction, RLC A, leaves the Accumulator holding the value 8BH (10001011B) with the carry set.

| Bytes: | 1 |
| Cycles: | 1 |
| Encoding: | 0 0 1 1 0 0 1 1 |

**Operation:**
\[
\begin{align*}
(An+1) &\leftarrow (An) && n = 0-6 \\
(A0) &\leftarrow (C) \\
(C) &\leftarrow (A7)
\end{align*}
\]

RR A

**Function:**
Rotate Accumulator Right

**Description:**
The eight bits in the Accumulator are rotated one bit to the right. Bit 0 is rotated into the bit 7 position. No flags are affected.

**Example:**
The Accumulator holds the value 0C5H (11000101B). The instruction, RR A, leaves the Accumulator holding the value 0E2H (11100010B) with the carry unaffected.

| Bytes: | 1 |
| Cycles: | 1 |
| Encoding: | 0 0 0 0 0 0 1 1 |

**Operation:**
\[
\begin{align*}
(An) &\leftarrow (An+1) && n = 0 - 6 \\
(A7) &\leftarrow (A0)
\end{align*}
\]

RRC A

**Function:**
Rotate Accumulator Right through the Carry flag

**Description:**
The eight bits in the Accumulator and the carry flag are together rotated one bit to the right. Bit 0 moves into the carry flag; the original value of the carry flag moves into the bit 7 position. No other flags are affected.

**Example:**
The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction, RRC A, leaves the Accumulator holding the value 62H (01100010B) with the carry set.

| Bytes: | 1 |
| Cycles: | 1 |
| Encoding: | 0 0 0 1 0 0 1 1 |

**Operation:**
\[
\begin{align*}
(An+1) &\leftarrow (An) && n = 0-6 \\
(A7) &\leftarrow (C) \\
(C) &\leftarrow (A0)
\end{align*}
\]
SETB <bit>

**Function:** Set bit

**Description:** SETB sets the indicated bit to one. SETB can operate on the carry flag or any directly addressable bit. No other flags are affected.

**Example:** The carry flag is cleared. Output Port 1 has been written with the value 34H (00110100B). The instructions,

```
SETB C
SETB P1.0
```

will leave the carry flag set to 1 and change the data output on Port 1 to 35H (00110101B).

**SETB C**

| Bytes: | 1 |
| Cycles: | 1 |
| Encoding: | ![Encoding](1 1 0 1 0 0 1 1) |
| Operation: | SETB \( (C) \leftarrow 1 \) |

**SETB bit**

| Bytes: | 2 |
| Cycles: | 1 |
| Encoding: | ![Encoding](1 1 0 1 0 0 1 0) |
| Operation: | SETB \( (bit) \leftarrow 1 \) |

**SJMP rel**

**Function:** Short Jump

**Description:** Program control branches unconditionally to the address indicated. The branch destination is computed by adding the signed displacement in the second instruction byte to the PC, after incrementing the PC twice. Therefore, the range of destinations allowed is from 128 bytes preceding this instruction to 127 bytes following it.

**Example:** The label “RELADR” is assigned to an instruction at program memory location 0123H. The instruction,

```
SJMP RELADR
```

will assemble into location 0100H. After the instruction is executed, the PC will contain the value 0123H.

*(Note: Under the above conditions the instruction following SJMP will be at 102H. Therefore, the displacement byte of the instruction will be the relative offset \((0123H - 0102H) = 21H.\)*

Put another way, an SJMP with a displacement of 0FEH would be an one-instruction infinite loop.

| Bytes: | 2 |
| Cycles: | 2 |
| Encoding: | ![Encoding](1 0 0 0 0 0 0 0) |
| Operation: | SJMP \( (PC) \leftarrow (PC) + 2 \), \( (PC) \leftarrow (PC) + \text{rel} \) |
SUBB A, <src-byte>

**Function:** Subtract with borrow

**Description:** SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set before executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision subtraction, so the carry is subtracted from the Accumulator along with the source operand). AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6.

When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number.

The source operand allows four addressing modes: register, direct, register-indirect, or immediate.

**Example:** The Accumulator holds 0C9H (11001001B), register 2 holds 54H (01010100B), and the carry flag is set. The instruction,

```assembly
SUBB A, R2
```

will leave the value 74H (01110100B) in the accumulator, with the carry flag and AC cleared but OV set.

Notice that 0C9H minus 54H is 75H. The difference between this and the above result is due to the carry (borrow) flag being set before the operation. If the state of the carry is not known before starting a single or multiple-precision subtraction, it should be explicitly cleared by a CLR C instruction.

### SUBB A, Rn

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**

```
1 0 0 1 1 r r r
```

- **Operation:**

```
SUBB (A) (A) (A) (C) (Rn)
```

### SUBB A, direct

- **Bytes:** 2
- **Cycles:** 1
- **Encoding:**

```
1 0 0 1 0 1 0 1
```

- **Operation:**

```
SUBB (A) (A) (C) (Rn)
```

### SUBB A, @Ri

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**

```
1 0 0 1 0 1 1 1
```

- **Operation:**

```
SUBB (A) (A) (C) (Ri)
```
SWAP A

Function: Swap nibbles within the Accumulator

Description: SWAP A interchanges the low- and high-order nibbles (four-bit fields) of the Accumulator (bits 3-0 and bits 7-4). The operation can also be thought of as a four-bit rotate instruction. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction, SWAP A leaves the Accumulator holding the value 5CH (01011100B).

Bytes: 1
Cycles: 1
Encoding: 1 1 0 0 0 1 0 0
Operation: SWAP (A) ← (A3-0) ↔ (A7-4)

XCH A, <byte>

Function: Exchange Accumulator with byte variable

Description: XCH loads the Accumulator with the contents of the indicated variable, at the same time writing the original Accumulator contents to the indicated variable. The source/destination operand can use register, direct, or register-indirect addressing.

Example: R0 contains the address 20H. The Accumulator holds the value 3FH (00111111B). Internal RAM location 20H holds the value 75H (01110101B). The instruction, XCH A, @R0 will leave RAM location 20H holding the values 3FH (00111111B) and 75H (01110101B) in the accumulator.

XCH A, Rn

Bytes: 1
Cycles: 1
Encoding: 1 1 0 0 1 0 0 0
Operation: XCH (A) ← (Rn)

XCH A, direct

Bytes: 2
Cycles: 1
Encoding: 1 1 0 0 0 1 0 1
Operation: XCH (A) ← (direct)
**XCH A, @Ri**

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**
  
<table>
<thead>
<tr>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
</table>
- **Operation:** XCH
  
  \[(A) \leftrightarrow ((Ri))\]

**XCHD A, @Ri**

- **Function:** Exchange Digit
- **Description:** XCHD exchanges the low-order nibble of the Accumulator (bits 3-0), generally representing a hexadecimal or BCD digit, with that of the internal RAM location indirectly addressed by the specified register. The high-order nibbles (bits 7-4) of each register are not affected. No flags are affected.
- **Example:** R0 contains the address 20H. The Accumulator holds the value 36H (00110110B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

  \[
  \text{XCHD } A, @R0
  \]

  will leave RAM location 20H holding the value 76H (01110110B) and 35H (00110101B) in the accumulator.

- **Bytes:** 1
- **Cycles:** 1
- **Encoding:**
  
<table>
<thead>
<tr>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
</table>
- **Operation:** XCHD
  
  \[(A_{3-0}) \leftrightarrow (Ri_{3-0})\]

**XRL <dest-byte>, <src-byte>**

- **Function:** Logical Exclusive-OR for byte variables
- **Description:** XRL performs the bitwise logical Exclusive-OR operation between the indicated variables, storing the results in the destination. No flags are affected.
  
  The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data. (Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.)
- **Example:** If the Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) then the instruction,

  \[
  \text{XRL } A, R0
  \]

  will leave the Accumulator holding the value 69H (01101001B).
  
  When the destination is a directly addressed byte, this instruction can complement combination of bits in any RAM location or hardware register. The pattern of bits to be complemented is then determined by a mask byte, either a constant contained in the instruction or a variable computed in the Accumulator at run-time. The instruction,

  \[
  \text{XRL } P1, \#00110001B
  \]

  will complement bits 5, 4 and 0 of output Port 1.
XRL  A, Rn
    Bytes: 1
    Cycles: 1
    Encoding: 0 1 1 0 1 r r r
    Operation: XRL  
               (A) ← (A) ^ (Rn)

XRL  A, direct
    Bytes: 2
    Cycles: 1
    Encoding: 0 1 1 0 0 1 0 1  
               direct address
    Operation: XRL  
               (A) ← (A) ^ (direct)

XRL  A, @Ri
    Bytes: 1
    Cycles: 1
    Encoding: 0 1 1 0 0 1 1 i
    Operation: XRL  
               (A) ← (A) ^ (@Ri)

XRL  A, #data
    Bytes: 2
    Cycles: 1
    Encoding: 0 1 1 0 0 1 0 0  
               immediate data
    Operation: XRL  
               (A) ← (A) ^ #data

XRL  direct, A
    Bytes: 2
    Cycles: 1
    Encoding: 0 1 1 0 0 0 1 0  
               direct address
    Operation: XRL  
               (direct) ← (direct) ^ (A)

XRL  direct, #data
    Bytes: 3
    Cycles: 2
    Encoding: 0 1 1 0 0 0 1 1  
               direct address  
               immediate data
    Operation: XRL  
               (direct) ← (direct) ^ # data
Chapter 6  Interrupt

There are 10 interrupt vector addresses available in STC12C5A60S2. Associating with each interrupt vector, the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the registers IE, CCON and IE2. These registers also contains a global disable bit (EA), which can be cleared to disable all interrupts at once.

Each interrupt source has two corresponding bits to represent its priority. One is located in SFR named IPH and other in IP register. Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. The following table shows the internal polling sequence in the same priority level and the interrupt vector address.

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>Vector address</th>
<th>Priority within level</th>
<th>Interrupt Priority setting(IPH, IP)</th>
<th>Priority 0 (lowest)</th>
<th>Priority 1</th>
<th>Priority 2</th>
<th>Priority 3 (highest)</th>
<th>Interrupt Request</th>
<th>Interrupt Enable Control Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>External interrupt 0</td>
<td>0003H</td>
<td>0(highest)</td>
<td>PX0H,PX0</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>IE0</td>
<td>EX0/EA</td>
</tr>
<tr>
<td>Timer 0</td>
<td>000BH</td>
<td>1</td>
<td>PT0H,PT0</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>TF0</td>
<td>ET0/EA</td>
</tr>
<tr>
<td>External interrupt 1</td>
<td>0013H</td>
<td>2</td>
<td>PX1H,PX1</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>IE1</td>
<td>EX1/EA</td>
</tr>
<tr>
<td>Timer1</td>
<td>001BH</td>
<td>3</td>
<td>PT1H,PT1</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>TF1</td>
<td>ET1/EA</td>
</tr>
<tr>
<td>Serial Port</td>
<td>0023H</td>
<td>4</td>
<td>PSH,PS</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>RI+TI</td>
<td>ES/EA</td>
</tr>
<tr>
<td>ADC</td>
<td>002BH</td>
<td>5</td>
<td>PADCH,PADC</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>ADC_FLAG</td>
<td>EADC/EA</td>
</tr>
<tr>
<td>LVD</td>
<td>0033H</td>
<td>6</td>
<td>PLVDH,PLVD</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>LVD</td>
<td>ELVD/EA</td>
</tr>
<tr>
<td>PCA</td>
<td>003BH</td>
<td>7</td>
<td>PPCAH,PPCA</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>CF+CCF0 + CCF1</td>
<td>(ECF+ECCF0 +ECCF1)/EA</td>
</tr>
<tr>
<td>UART2 (S2)</td>
<td>0043H</td>
<td>8</td>
<td>PS2H,PS2</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>S2TI+S2RI</td>
<td>ES2/EA</td>
</tr>
<tr>
<td>SPI</td>
<td>004BH</td>
<td>9</td>
<td>PSPIH,PSPI</td>
<td>0,0</td>
<td>0,1</td>
<td>1,0</td>
<td>1,1</td>
<td>SPIF</td>
<td>ESPI/EA</td>
</tr>
</tbody>
</table>
6.1 Interrupt Structure

STC12C5A60S2 Interrupt system diagram
The External Interrupts INT0 and INT1 can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to if and only if the interrupt was transition-activated, otherwise the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer 0 and Timer1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers in most cases. When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI and TI that generated the interrupt, and the bit will have to be cleared by software.

The ADC interrupt is generated by the flag – ADC_FLAG. It should be cleared by software.

The Low Voltage Detect interrupt is generated by the flag – LVDF(PCON.5) in PCON register. It should be cleared by software.

The PCA interrupt is generated by the logical OR of CF, CCF0 ~ CCF1. The service routine should poll CF and CCF0 ~ CCF1 to determine which one to request service and it will be cleared by software.

The secondary serial port interrupt is generated by the logical OR of S2RI and S2TI. Neither of these flags is cleared by hardware when the service routine is vectored to. The service routine should poll S2RI and S2TI to determine which one to request service and it will be cleared by software.

The SPI interrupt is generated by the flag SPIF. It can only be cleared by writing a “1” to SPIF bit in software.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. In other words, interrupts can be generated or pending interrupts can be canceled in software.
## 6.2 Interrupt Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Bit Address and Symbol</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE</td>
<td>Interrupt Enable</td>
<td>A8H</td>
<td>EA ELVD EADC ES ET1 EX1 ET0 EX0</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IP</td>
<td>Interrupt Priority Low</td>
<td>B8H</td>
<td>PPCA PLVD PADC PS PT1 PX1 PT0 PX0</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IPH</td>
<td>Interrupt Priority High</td>
<td>B7H</td>
<td>PPCAH PLVDH PADCHE PSH PT1H PX1H PT0H PX0H</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IE2</td>
<td>Interrupt Enable 2</td>
<td>AFH</td>
<td>- - - - - - ESPI ES2</td>
<td>xxxx xx00B</td>
</tr>
<tr>
<td>IP2</td>
<td>2nd Interrupt Priority Low register</td>
<td>B5H</td>
<td>- - - - - - SPSI SPS2</td>
<td>xxxx xx00B</td>
</tr>
<tr>
<td>IP2H</td>
<td>2nd Interrupt Priority Low register</td>
<td>B6H</td>
<td>- - - - - - SPSIH SPS2H</td>
<td>xxxx xx00B</td>
</tr>
<tr>
<td>TCON</td>
<td>Timer Control</td>
<td>88H</td>
<td>TF1 TR1 TF0 TR0 IE1 IT1 IE0 IT0</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>SCON</td>
<td>Serial Control</td>
<td>98H</td>
<td>SM0/FE SM1 SM2 REN TB8 RB8 T1 R1</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>AUXR</td>
<td>Auxiliary register</td>
<td>8EH</td>
<td>T0x12 T1x12 UART_M0x6 BRTR S2SMOD BRTx12 EXTRAM S1BR5</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>PCON</td>
<td>Power Control</td>
<td>87H</td>
<td>SMOD SMOD0 LVDF POF GF1 GF0 PD IDL</td>
<td>0001 0000B</td>
</tr>
<tr>
<td>WAKE_CLKO</td>
<td>CLK_Output Power down Wake-up control register</td>
<td>8FH</td>
<td>PCAWAKEU RXD_PIN_IE T1_PIN_IE T0_PIN_IE LVD_WAKE BRTCLKO T1CLKO T0CLKO</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>ADC_CONTR</td>
<td>ADC Control</td>
<td>B8H</td>
<td>ADC_POWER SPEED1 SPEED0 ADC_FLAG ADC_START CHS2 CHS1 CHS0</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>CCON</td>
<td>PCA Control Register</td>
<td>D8H</td>
<td>CF CR - - - - CCF1 CCF0</td>
<td>00xx xx00B</td>
</tr>
<tr>
<td>CMOD</td>
<td>PCA Mode Register</td>
<td>D9H</td>
<td>CIDL - - - - CPS2 CPS1 CPS0 ECF</td>
<td>00xx 0000B</td>
</tr>
<tr>
<td>CCAPM0</td>
<td>PCA Module 0 Mode Register</td>
<td>DAH</td>
<td>-</td>
<td>ECOM0 CAP00 CAPN0 MAT0 TOG0 PWM0 ECCF0</td>
</tr>
<tr>
<td>CCAPM1</td>
<td>PCA Module 1 Mode Register</td>
<td>DBH</td>
<td>-</td>
<td>ECOM1 CAP11 CAPN1 MAT1 TOG1 PWM1 ECCF1</td>
</tr>
</tbody>
</table>
### IE: Interrupt Enable Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EA</td>
<td>IE.7</td>
<td>Enables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.</td>
</tr>
<tr>
<td>ELVD</td>
<td>IE.6</td>
<td>Low voltage detection interrupt enable bit.</td>
</tr>
<tr>
<td>EADC</td>
<td>IE.5</td>
<td>ADC interrupt enable bit.</td>
</tr>
<tr>
<td>ES</td>
<td>IE.4</td>
<td>Serial Port interrupt enable bit.</td>
</tr>
<tr>
<td>ET1</td>
<td>IE.3</td>
<td>Timer 1 interrupt enable bit.</td>
</tr>
<tr>
<td>EX1</td>
<td>IE.2</td>
<td>External interrupt 1 enable bit.</td>
</tr>
<tr>
<td>ET0</td>
<td>IE.1</td>
<td>Timer 0 interrupt enable bit.</td>
</tr>
<tr>
<td>EX0</td>
<td>IE.0</td>
<td>External interrupt 0 enable bit.</td>
</tr>
</tbody>
</table>

### IP: Interrupt Priority Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPCA</td>
<td>IP.7</td>
<td>PCA interrupt priority bit.</td>
</tr>
<tr>
<td>PLVD</td>
<td>IP.6</td>
<td>Low voltage detection interrupt priority.</td>
</tr>
<tr>
<td>PADC</td>
<td>IP.5</td>
<td>ADC interrupt priority bit.</td>
</tr>
<tr>
<td>PS</td>
<td>IP.4</td>
<td>Serial Port interrupt priority bit.</td>
</tr>
<tr>
<td>PT1</td>
<td>IP.3</td>
<td>Timer 1 interrupt priority bit.</td>
</tr>
<tr>
<td>PX1</td>
<td>IP.2</td>
<td>External interrupt 1 priority bit.</td>
</tr>
<tr>
<td>PT0</td>
<td>IP.1</td>
<td>Timer 0 interrupt priority bit.</td>
</tr>
<tr>
<td>PX0</td>
<td>IP.0</td>
<td>External interrupt 0 priority bit.</td>
</tr>
</tbody>
</table>
**Auxiliary Interrupt Enable register (IE2)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B7-B2</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESPI</td>
<td>When set, enables SPI interrupt.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ES2</td>
<td>When set, enables UART2 interrupt.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Interrupt Priority Low register 2(IP2)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>B7-B2</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSPI</td>
<td>SPI interrupt priority bit.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PS2</td>
<td>UART2 interrupt priority bit.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Interrupt Priority High register(IPH)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>PPCAH</td>
<td>PLVDH</td>
<td>PADCH</td>
<td>PSH</td>
<td>PT1H</td>
<td>PX1H</td>
<td>PT0H</td>
<td>PX0H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PPCAH</td>
<td>When set, set priority for PCA interrupt higher.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLVDH</td>
<td>When set, set priority for Low Voltage interrupt higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PADCH</td>
<td>When set, set priority for ADC interrupt higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSH</td>
<td>When set, set priority for serial port interrupt higher(UART)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT1H</td>
<td>When set, set priority for Timer 1 interrupt higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PX1H</td>
<td>When set, set priority for external interrupt 1 higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT0H</td>
<td>When set, set priority for Timer 0 interrupt higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PX0H</td>
<td>When set, set priority for external interrupt 0 higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Interrupt Priority High register 2(IP2H)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSPIH</td>
<td>When set, set priority for SPI interrupt higher</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PS2H</td>
<td>When set, set priority for the secondary UART interrupt higher(UART2)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IPxH and IPx are used to form 4-level priority interrupt as the following table.

<table>
<thead>
<tr>
<th>{IPxH,IPx}</th>
<th>Priority Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1 (highest)</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>
## TCON register: Timer/Counter Control Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Position</th>
<th>Name and Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>TF1</td>
<td>TCON.7</td>
<td>Timer 1 overflow Flag. Set by hardware on Timer/Counter overflow. cleared by hardware when processor vectors to interrupt routine.</td>
</tr>
<tr>
<td>TR1</td>
<td>TCON.6</td>
<td>Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.</td>
</tr>
<tr>
<td>TF0</td>
<td>TCON.5</td>
<td>Timer 0 overflow Flag. Set by hardware on Timer/Counter overflow. cleared by hardware when processor vectors to interrupt routine.</td>
</tr>
<tr>
<td>TR0</td>
<td>TCON.4</td>
<td>Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.</td>
</tr>
<tr>
<td>IE1</td>
<td>TCON.3</td>
<td>Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.</td>
</tr>
<tr>
<td>IT1</td>
<td>TCON.2</td>
<td>Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.</td>
</tr>
<tr>
<td>IE0</td>
<td>TCON.1</td>
<td>Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.</td>
</tr>
<tr>
<td>IT0</td>
<td>TCON.0</td>
<td>Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.</td>
</tr>
</tbody>
</table>

## SCON register

<table>
<thead>
<tr>
<th>bit name</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>description</td>
<td>SM0/FE</td>
<td>SM1</td>
<td>SM2</td>
<td>REN</td>
<td>TB8</td>
<td>RB8</td>
<td>TI</td>
<td>RI</td>
</tr>
</tbody>
</table>

- **FE**: Framing Error bit. The SMOD0 bit must be set to enable access to the FE bit.
  - 0: The FE bit is not cleared by valid frames but should be cleared by software.
  - 1: This bit set by the receiver when an invalid stop bit id detected.

- **SM0,SM1**: Serial Port Mode Bit 0/1.
  - 0: 8-bit shift register SYScclk/12
  - 1: 8-bit UART variable

- **SM2**: Enable the automatic address recognition feature in mode 2 and 3. If SM2=1, RI will not be set unless the received 9th data bit is 1, indicating an address, and the received byte is a Given or Broadcast address. In mode1, if SM2=1 then RI will not be set unless a valid stop Bit was received, and the received byte is a Given or Broadcast address. In mode 0, SM2 should be 0.

- **REN**: When set enables serial reception.

- **TB8**: The 9th data bit which will be transmitted in mode 2 and 3.

- **RB8**: In mode 2 and 3, the received 9th data bit will go into this bit.

- **TI**: Transmit interrupt flag.

- **RI**: Receive interrupt flag.
PCON: Power Control register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
<td>IDL</td>
</tr>
</tbody>
</table>

SMOD: double baud rate control bit.
0: Disable double baud rate of the UART.
1: Enable double baud rate of the UART in mode 1, 2, or 3.

SMOD0: Frame Error select.
0: SCON.7 is SM0 function.
1: SCON.7 is FE function. Note that FE will be set after a frame error regardless of the state of SMOD0.

LVDF: Pin Low-Voltage Flag. Once low voltage condition is detected (VCC power is lower than LVD voltage), it is set by hardware (and should be cleared by software).

POF: Power-On flag. It is set by power-off-on action and can only cleared by software.

GF1: General-purposed flag 1

GF0: General-purposed flag 0

PD: Power-Down bit.

IDL: Idle mode bit.

WAKE_CLKO register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>PCA_WAKEUP</td>
<td>RXD_PIN_IE</td>
<td>T1_PIN_IE</td>
<td>T0_PIN_IE</td>
<td>LVD_WAKE</td>
<td>BRTCKLO</td>
<td>T1CKLO</td>
<td>T0CKLO</td>
</tr>
</tbody>
</table>

PCAWAKEUP: When set and the associated-PCA interrupt control registers is configured correctly, the CEXn pin of PCA function is enabled to wake up MCU from power-down state.

RXD_PIN_IE: When set and the associated-UART interrupt control registers is configured correctly, the RXD pin (P3.0) is enabled to wake up MCU from power-down state.

T1_PIN_IE: When set and the associated-Timer1 interrupt control registers is configured correctly, the T1 pin (P3.5) is enabled to wake up MCU from power-down state.

T0_PIN_IE: When set and the associated-Timer0 interrupt control registers is configured correctly, the T1 pin (P3.4) is enabled to wake up MCU from power-down state.

LVD_WAKE: When set and the associated-LVD interrupt control registers is configured correctly, the CMPIN pin is enabled to wake up MCU from power-down state.

BRTCKLO: When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRG overflow rate divided by 2.

T1CKLO: When set, P3.5 is enabled to be the clock output of Timer 1. The clock rate is Timer 1 overflow rate divided by 2.

T0CKLO: When set, P3.4 is enabled to be the clock output of Timer 0. The clock rate is Timer 0 overflow rate divided by 2.

ADC_CONTR: AD Control register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>ADC_POWER</td>
<td>SPEED1</td>
<td>SPEED0</td>
<td>ADC_FLAG</td>
<td>ADC_START</td>
<td>CHS2</td>
<td>CHS1</td>
<td>CHS0</td>
</tr>
</tbody>
</table>

ADC_POWER(ADC_CONTR.7): When clear, shut down the power of ADC block. When set, turn on the power of ADC block.

ADC_FLAG(ADC_CONTR.4): ADC interrupt flag.
CCON register

<table>
<thead>
<tr>
<th>bit</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CF</td>
<td>CR</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CCF1</td>
</tr>
<tr>
<td></td>
<td>CCF0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CF : PCA Counter Overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.

CR : PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.

CCF1: PCA Module 1 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

CCF0 : PCA Module 0 interrupt flag. Set by hardware when a match or capture occurs. Must be cleared by software.

CMOD register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CIDL</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CPS2</td>
<td>CPS1</td>
<td>CPS0</td>
<td>ECF</td>
</tr>
</tbody>
</table>

CIDL : Counter Idle control. CIDL=0 programs the PCA Counter to continue functioning during idle mode. CIDL=1 programs it to be gated off during idle.

CPS2 ~ CPS0 : PCA Counter Pulse Select bits.
0 0 0  Internal clock, fosc/12
0 0 1  Internal clock, fosc/2
0 1 0  Timer 0 overflow
0 1 1  External clock at ECI/P1.2 pin
1 0 0  Internal clock, fosc
1 0 1  Internal clock, fosc/4
1 1 0  Internal clock, fosc/6
1 1 1  Internal clock, fosc/8

ECF : PCA Enable Counter Overflow interrupt. ECF=1 enables CF bit in CCON to generate an interrupt.

CCAPMn register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>ECOMn</td>
<td>CAPPn</td>
<td>CAPNn</td>
<td>MATn</td>
<td>TOGn</td>
<td>PWMn</td>
<td>ECCFn</td>
</tr>
</tbody>
</table>

ECOMn : Enable Comparator. ECOMn=1 enables the comparator function.

CAPPn : Capture Positive, CAPPn=1 enables positive edge capture.

CAPNn : Capture Negative, CAPNn=1 enables negative edge capture.

MATn : Match. When MATn=1, a match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set.

TOGn : Toggle. When TOGn=1, a match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.

PWMn : Pulse Width Modulation. PWMn=1 enables the CEXn pin to be used as a pulse width modulated output.

ECCFn : Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate
6.3 Interrupt Priorities

Each interrupt source can also be individually programmed to one of four priority levels by setting or clearing the bits in Special Function Registers IP or IP2 and IPH or IP2H. A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can’t be interrupted by any other interrupt source.

If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence, as follows:

<table>
<thead>
<tr>
<th>Source</th>
<th>Priority Within Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.</td>
<td>IE0</td>
</tr>
<tr>
<td>1.</td>
<td>TF0</td>
</tr>
<tr>
<td>2.</td>
<td>IE1</td>
</tr>
<tr>
<td>3.</td>
<td>TF1</td>
</tr>
<tr>
<td>4.</td>
<td>RI +TI</td>
</tr>
<tr>
<td>5.</td>
<td>ADC_FLAG</td>
</tr>
<tr>
<td>6.</td>
<td>LVDF</td>
</tr>
<tr>
<td>7.</td>
<td>PCA</td>
</tr>
<tr>
<td>8.</td>
<td>S2RI+S2TI</td>
</tr>
<tr>
<td>9.</td>
<td>SPIF</td>
</tr>
</tbody>
</table>

Note that the “priority within level” structure is only used to resolve simultaneous requests of the same priority level.

6.4 How Interrupts Are Handled

External interrupt pins and other interrupt sources are sampled at the rising edge of each instruction Opcode fetch cycle. The samples are polled during the next instruction Opcode fetch cycle. If one of the flags was in a set condition of the first cycle, the second cycle of polling cycles will find it and the interrupt system will generate an hardware LCALL to the appropriate service routine as long as it is not blocked by any of the following conditions.

Block conditions:

- An interrupt of equal or higher priority level is already in progress.
- The current cycle (polling cycle) is not the final cycle in the execution of the instruction in progress.
- The instruction in progress is RETI or any write to the IE, IE2, IP, IP2, IPH and IP2H registers.
- The ISP/IAP activity is in progress.

Any of these four conditions will block the generation of the hardware LCALL to the interrupt service routine. Condition 2 ensures that the instruction in progress will be completed before vectoring into any service routine. Condition 3 ensures that if the instruction in progress is RETI or any access to IE, IE2, IP, IP2, IPH or IP2H, then at least one or more instruction will be executed before any interrupt is vectored to.

The polling cycle is repeated with the last clock cycle of each instruction cycle. Note that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the fact that the interrupt flag was once active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. The interrupt flag was once active but not serviced is not kept in memory. Every polling cycle is new.
Note that if an interrupt of higher priority level goes active prior to the rising edge of the third machine cycle, then in accordance with the above rules it will be vectored to during fifth and sixth machine cycle, without any instruction of the lower priority routine having been executed.

Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn’t. It never clears the Serial Port flags. This has to be done in the user’s software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown be low.

<table>
<thead>
<tr>
<th>Source</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE0</td>
<td>0003H</td>
</tr>
<tr>
<td>TF0</td>
<td>000BH</td>
</tr>
<tr>
<td>IE1</td>
<td>0013H</td>
</tr>
<tr>
<td>TF1</td>
<td>001BH</td>
</tr>
<tr>
<td>RI+TI</td>
<td>0023H</td>
</tr>
<tr>
<td>ADC_FLAG</td>
<td>002BH</td>
</tr>
<tr>
<td>LVDF</td>
<td>0033H</td>
</tr>
<tr>
<td>PCA</td>
<td>003BH</td>
</tr>
<tr>
<td>S2RI+S2TI</td>
<td>0043H</td>
</tr>
<tr>
<td>SPIF</td>
<td>004BH</td>
</tr>
</tbody>
</table>

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

### 6.5 External Interrupts

The external sources can be programmed to be level-activated or transition-activated by clearing or setting bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the INTx pin. If ITx=1, external interrupt x is edge-triggered. In this mode if successive samples of the INTx pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 system clocks to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one machine cycle, and then hold it low for at least one machine cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.
Example: Design an intrusion warning system using interrupts that sounds a 400Hz tone for 1 second (using a loudspeaker connected to P1.7) whenever a door sensor connected to INT0 makes a high-to-low transition.

Assembly Language Solution

```
ORG 0
LJMP MAIN ;3-byte instruction
LJMP INT0INT ;EXT 0 vector address
ORG 000BH ;Timer 0 vector
LJMP T0INT
ORG 001BH ;Timer 1 vector
LJMP T1INT
ORG 0030H

MAIN:
    SETB IT0 ;negative edge activated
    MOV TMOD, #11H ;16-bit timer mode
    MOV IE, #81H ;enable EXT 0 only
    SJMP $ ;now relax

; INT0INT:
    MOV R7, #20 ;20 ' 5000 us = 1 second
    SETB TF0 ;force timer 0 interrupt
    SETB TF1 ;force timer 1 interrupt
    SETB ET0 ;begin tone for 1 second
    SETB ET1 ;enable timer interrupts
    RETI

; T0INT:
    CLR TR0 ;stop timer
    DJNZ R7, SKIP ;if not 20th time, exit
    CLR ET0 ;if 20th, disable tone
    CLR ET1 ;disable itself
    LJMP EXIT

SKIP:
    MOV TH0, #HIGH (-50000) ;0.05sec. delay
    MOV TL0, #LOW (-5000)
    EXIT:
    RETI

; T1INT:
    CLR TR1
    MOV TH1, #HIGH (-1250) ;count for 400Hz
    MOV TL1, #LOW (-1250)
    CPL P1.7 ;music maestro!
    SETB TR1
    RETI
END
```
C Language Solution

```
#include <REG51.H>  /* SFR declarations */
sbit outbit = P1^7;  /* use variable outbit to refer to P1.7 */
unsigned char R7;   /* use 8-bit variable to represent R7 */

main()
{
    IT0 = 1;                   /* negative edge activated */
    TMOD = 0x11;               /* 16-bit timer mode */
    IE = 0x81;                 /* enable EXT 0 only */
    while(1);
}

void INT0INT(void)  interrupt 0
{
    R7 = 20;                   /* 20 x 5000us = 1 second */
    TF0 = 1;                   /* force timer 0 interrupt */
    TF1 = 1;                   /* force timer 1 interrupt */
    ET0 = 1;                   /* begin tone for 1 second */
    ET1 = 1;                   /* enable timer 1 interrupts */
    /* timer interrupts will do the work */
}

void T0INT(void)  interrupt 1
{
    TR0 = 0;                   /* stop timer */
    R7 = R7-1;                 /* decrement R7 */
    if (R7 == 0)               /* if 20th time, */
    {
        ET0 = 0;                 /* disable itself */
        ET1 = 0;
    }
    else
    {
        TH0 = 0x3C;               /* 0.05 sec. delay */
        TL0 = 0xB0;
    }
}

void T1INT (void) interrupt 3
{
    TR0 = 0;
    TH1 = 0xFB;               /* count for 400Hz */
    TL1 = 0x1E;
    outbit = !outbit;      /* music maestro! */
    TR1 = 1;
}
```
In the above assembly language solution, five distinct sections are the interrupt vector locations, the main program, and the three interrupt service routines. All vector locations contain LJMP instructions to the respective routines. The main program, starting at code address 0030H, contains only four instructions. SETB IT0 configures the door sensing interrupt input as negative-edge triggered. MOV TMOD, #11H configures both timers for mode 1, 16-bit timer mode. Only the external 0 interrupt is enabled initially (MOV IE,#81H), so a "door-open" condition is needed before any interrupt is accepted. Finally, SJMP $ puts the main program in a do-nothing loop.

When a door-open condition is sensed (by a high-to-low transition of INT0), an external 0 interrupt is generated, INT0INT begins by putting the constant 20 in R7, then sets the overflow flags for both timers to force timer interrupts to occur.

Timer interrupt will only occur, however, if the respective bits are enabled in the IE register. The next two instructions (SETB ET0 and SETB ET1) enable timer interrupts. Finally, INT0INT terminates with a RETI to the main program.

Timer 0 creates the 1 second timeout, and Timer 1 creates the 400Hz tone. After INT0INT returns to the main program, timer interrupt are immediately generated (and accepted after one execution of SJMP $). Because of the fixed polling sequence, the Timer 0 interrupt is serviced first. A 1 second timeout is created by programming 20 repetitions of a 50,000 us timeout. R7 serves as the counter. Nineteen times out of 20, T0INT operates as follows. First, Timer 0 is turned off and R7 is decremented. Then, TH0/TL is reloaded with -50,000, the timer is turned back on, and the interrupt is terminated. On the 20th Timer 0 interrupt, R7 is decremented to 0 (1 second has elapsed). Both timer interrupts are disabled (CLR ET0, CLR ET1) and the interrupt is terminated. No further timer interrupts will be generated until the next "door-open" condition is sensed.

The 400Hz tone is programmed using Timer 1 interrupts, 400Hz requires a period of 1/400 = 2,500 us or 1,250 high-time and 1,250 us low-time. Each timer 1 ISR simply puts -1250 in TH1/TL1, complements the port bit driving the loudspeaker, then terminates.
6.6 External Interrupt 0 Demo Programs

1. C program

/*-----------------------------------*/
/* --- STC MCU International Limited -----------------------------------*/
/* --- STC 1T Series MCU Ext0(Falling edge) Demo -------------------*/
/* --- Mobile: (86)13922805190 ------------------------------------------*/
/* --- Fax: 86-755-82944243 ----------------------------------------------*/
/* --- Tel: 86-755-82948412 -------------------------------------------------*/
/* --- Web: www.STCMCU.com ---------------------------------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*--------------------------------------------------------------------------------------*/

#include "reg51.h"

//External interrupt0 service routine
void exint0() interrupt 0 //interrupt 0 (location at 0003H)
{
}

void main()
{
    IT0 = 1;            //set INT0 int type (1:Falling 0:Low level)
    EX0 = 1;            //enable INT0 interrupt
    EA = 1;             //open global interrupt switch

    while (1);
}
2. Assembly program

```assembly
; interrupt vector table
ORG 0000H
LJMP MAIN

ORG 0003H ; interrupt 0 (location at 0003H)
LJMP EXINT0

ORG 0100H
MAIN:
  MOV SP, #7FH ; initial SP
  SETB IT0 ; set INT0 int type (1: Falling 0: Low level)
  SETB EX0 ; enable INT0 interrupt
  SETB EA ; open global interrupt switch
  SJMP $

; External interrupt0 service routine

EXINT0:
  RETI

;-----------------------------------------

END
```
### 6.7 External Interrupt 1 Demo Programs

#### 1. C program

```c
#include "reg51.h"

//External interrupt1 service routine
void extint1() interrupt 2  //interrupt 1 (location at 0013H)
{
}

void main()
{
    IT1 = 1;   //set INT1 int type (1:Falling only 0:Low level)
    EX1 = 1;   //enable INT1 interrupt
    EA = 1;    //open global interrupt switch

    while (1);
}
```

---

If you want to use the program or the program referenced in the article, please specify in which data and procedures from STC.
2. Assembly program

; /************************************************************************
; /* .................................................................*/
; /* --- STC MCU International Limited ----------------------------*/
; /* --- STC 1T Series MCU Ext1 (Falling edge) Demo ---------------*/
; /* --- Mobile: (86)13922805190 -----------------------------------*/
; /* --- Fax: 86-755-82944243 --------------------------------------*/
; /* --- Tel: 86-755-82948412 ----------------------------------------*/
; /* --- Web: www.STCMCU.com --------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; /************************************************************************

;-----------------------------------------
;interrupt vector table

ORG     0000H
LJMP    MAIN

ORG     0013H                      ;interrupt 2 (location at 0013H)
LJMP    EXINT1

;-----------------------------------------

ORG     0100H
MAIN:

MOV      SP, #7FH                   ;initial SP
SETH     IT1                        ;set INT1 int type (1:Falling 0:Low level)
SETB     EX1                        ;enable INT1 interrupt
SETH     EA                         ;open global interrupt switch
SJMP     $

;-----------------------------------------

;External interrupt1 service routine

EXINT1:

RETI

;-----------------------------------------

END
6.8 Response Time

The INT0 and INT1 levels are inverted and latched into the interrupt flags IE0 and IE1 at rising edge of every system clock cycle.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set after which the timers overflow. The values are then polled by the circuitry at rising edge of the next system clock cycle.

If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes six system clock cycles. Thus, a minimum of seven complete system clock cycles elapse between activation of an external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would result if the request is blocked by one of the four previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt’s service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (LCALL) are only 6 cycles long, and if the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 6 cycles to complete the next instruction if the instruction is LCALL).

Thus, in a single-interrupt system, the response time is always more than 7 cycles and less than 12 cycles.
Chapter 7  Timer/Counter 0/1

Timer 0 and timer 1 are like the ones in the conventional 8051, both of them can be individually configured as timers or event counters.

In the “Timer” function, the register is incremented every 12 system clocks or every system clock depending on AUXR.7(T0x12) bit and AUXR.6(T1x12). In the default state, it is fully the same as the conventional 8051. In the x12 mode, the count rate equals to the system clock.

In the “Counter” function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once at the positive edge of every clock cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during at the end of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles(24 system clocks) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the system clock. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the “Timer” or “Counter” selection, Timer 0 and Timer 1 have four operating modes from which to select. The “Timer” or “Counter” function is selected by control bits C/T in the Special Function Register TMOD. These two Timer/Counter have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both Timer Counters. Mode 3 is different. The four operating modes are described in the following text.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Bit Address and Symbol</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCON</td>
<td>Timer Control</td>
<td>88H</td>
<td>TF1</td>
<td>TR1</td>
</tr>
<tr>
<td>TMOD</td>
<td>Timer Mode</td>
<td>89H</td>
<td>GATE</td>
<td>C/T</td>
</tr>
<tr>
<td>TL0</td>
<td>Timer Low 0</td>
<td>8AH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TL1</td>
<td>Timer Low 1</td>
<td>8BH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TH0</td>
<td>Timer High 0</td>
<td>8CH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TH1</td>
<td>Timer High 1</td>
<td>8DH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AUXR</td>
<td>Auxiliary register</td>
<td>8EH</td>
<td>T0x12</td>
<td>T1x12</td>
</tr>
<tr>
<td>WAKE_CLKO</td>
<td>CLK_Output</td>
<td>8FH</td>
<td>PCWAKE</td>
<td>RXD_PIN_IE</td>
</tr>
</tbody>
</table>
AUXR register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
<td>S2SMOD</td>
<td>BRTx12</td>
<td>EXTRAM</td>
<td>S1BRS</td>
</tr>
</tbody>
</table>

T0x12
0 : The clock source of Timer 0 is SYSclk/12.
1 : The clock source of Timer 0 is SYSclk/1.

T1x12
0 : The clock source of Timer 1 is SYSclk/12.
1 : The clock source of Timer 1 is SYSclk/1.

BRTx12
0 : The baud-rate generator is incremented every 12 system clocks.
1 : The baud-rate generator is incremented every system clock.

WAKE_CLKO:CLK_Output Power down Wake-up control register

<table>
<thead>
<tr>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>RXD_PIN_IE</td>
<td>T1_PIN_IE</td>
<td>T0_PIN_IE</td>
<td>LVD_WAKE</td>
<td>BRTCLKO</td>
<td>T1CLKO</td>
<td>T0CLKO</td>
</tr>
</tbody>
</table>

BRTCLKO : When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRT overflow rate divided by 2.

T1CLKO : When set, P3.5 is enabled to be the clock output of Timer 1. The clock rate is Timer1 overflow rate divided by 2.

T0CLKO : When set, P3.4 is enabled to be the clock output of Timer 0. The clock rate is Timer0 overflow rate divided by 2.

TMOD register : Timer/Counter Mode Control Register

<table>
<thead>
<tr>
<th>(MSB)</th>
<th>(LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GATE</td>
<td>C/T</td>
</tr>
<tr>
<td>Timer 1</td>
<td>Timer 0</td>
</tr>
</tbody>
</table>

GATE
Gating control when set. Timer/Counter "x" is enabled only while "INTx" pin is high and "TRx" control pin is set. When cleared Timer "x" is enabled whenever "TRx" control bit is set.

C/T
Timer or Counter Selector cleared for Timer operation (input from internal system clock). Set for Counter operation (input from "Tx" input pin).

M1  M0

<table>
<thead>
<tr>
<th>Operating Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
</tr>
<tr>
<td>0 1</td>
</tr>
<tr>
<td>1 0</td>
</tr>
<tr>
<td>1 1</td>
</tr>
<tr>
<td>1 1</td>
</tr>
</tbody>
</table>
7.1 Timer/Counter 0 Mode of Operation

Mode 0

In this mode, the timer 0 is configured as a 13-bit timer/counter. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE=0 or INT0 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT0, to facilitate pulse width measurements.) TR0 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 13-Bit register consists of all 8 bits of TH0 and the lower 5 bits of TL0. The upper 3 bits of TL0 are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

There are two different GATE bits. one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).
Mode 1

In this mode, the timer register is configured as a 16-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF0. The counted input is enabled to the timer when TR0 = 1 and either GATE = 0 or INT0 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT0, to facilitate pulse width measurements.) TR0 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 16-Bit register consists of all 8 bits of TH0 and the lower 8 bits of TL0. Setting the run flag (TR0) does not clear the registers.

Mode 1 is the same as Mode 0, except that the timer register is being run with all 16 bits.

There are two simple programs that demonstrates Timer 0 as 16-bit Timer/Counter, one written in C language while other in Assembly language.

C Program:

```c
#include "reg51.h"

typedef unsigned char BYTE;
typedef unsigned int WORD;

#include reg51.h

#define FOSC 18432000L
#define MODE1T                      //Timer clock mode, comment this line is 12T mode, uncomment is 1T mode
```

There are two simple programs that demostrates Timer 0 as 16-bit Timer/Counter, one written in C language while other in Assembly language.
/* define SFR */
sfr AUXR = 0x8e; //Auxiliary register
sbit TEST_LED = P0^0; //work LED, flash once per second

/* define variables */
WORD count; //1000 times counter

/*********************************************/

/* Timer0 interrupt routine */
void tm0_isr() interrupt 1 using 1
{
    TL0 = T1MS;  //reload timer0 low byte
    TH0 = T1MS >> 8;  //reload timer0 high byte
    if (count-- == 0)
    {
        count = 1000;  //reset counter
        TEST_LED = ! TEST_LED;  //work LED flash
    }
}

/*********************************************/

/* main program */
void main()
{
    #ifdef MODE1T
    AUXR = 0x80; //timer0 work in 1T mode
    #endif
    TMOD = 0x01; //set timer0 as mode1 (16-bit)
    TL0 = T1MS; //initial timer0 low byte
    TH0 = T1MS >> 8; //initial timer0 high byte
    TR0 = 1; //timer0 start running
    ET0 = 1; //enable timer0 interrupt
    EA = 1; //open global interrupt switch
    count = 0; //initial counter

    while (1); //loop
}
Assembly Program:

;*--------------------------------------------------------------*
;* --- STC MCU International Limited -------------------------------*
;* --- STC 1T Series 16-bit Timer Demo -----------------------------*
;* --- Mobile: (86)13922805190 ------------------------------------*
;* --- Fax: 86-755-82944243 ----------------------------------------*
;* --- Tel: 86-755-82948412 -----------------------------------------*
;* --- Web: www.STCMCU.com ----------------------------------------*
;* If you want to use the program or the program referenced in the  *
;* article, please specify in which data and procedures from STC    *
;*--------------------------------------------------------------*

;* define constants */
#define MODE1T ;Timer clock mode, comment this line is 12T mode, uncomment is 1T mode
#ifdef MODE1T
T1MS EQU 0B800H ;1ms timer calculation method in 1T mode is (65536-18432000/1000)
#else
T1MS EQU 0FA00H ;1ms timer calculation method in 12T mode is (65536-18432000/12/1000)
#endif

;* define SFR */
AUXR DATA 8EH ;Auxiliary register
TEST_LED BIT P1.0 ;work LED, flash once per second

;* define variables */
COUNT DATA 20H ;1000 times counter (2 bytes)

;-------------------------------
ORG 0000H
LJMP MAIN
ORG 000BH
LJMP TM0_ISR

;-------------------------------
;* main program */
MAIN:
#ifdef MODE1T
MOV AUXR, #80H ;timer0 work in 1T mode
#else
MOV TMOD, #01H ;set timer0 as mode1 (16-bit)
MOV TL0, #LOW T1MS ;initial timer0 low byte
MOV TH0, #HIGH T1MS ;initial timer0 high byte
SETB TR0 ;timer0 start running
SETB ET0 ;enable timer0 interrupt
SETB EA ;open global interrupt switch
CLR A
MOV COUNT, A
MOV COUNT+1, A ;initial counter
SJMP $
#endif

www.STCMCU.com Mobile:(86)13922805190 Tel:86-755-82948412 Fax:86-755-82944243
;-----------------------------
; /* Timer0 interrupt routine */
TM0_ISR:
        PUSH ACC
        PUSH PSW
        MOV TL0, #LOW T1MS         ;reload timer0 low byte
        MOV TH0, #HIGH T1MS        ;reload timer0 high byte
        MOV A, COUNT
        ORL A, COUNT+1             ;check whether count(2byte) is equal to 0
        JNZ SKIP
        MOV COUNT, #LOW 1000       ;1ms * 1000 -> 1s
        MOV COUNT+1, #HIGH 1000
        CPL TEST_LED               ;work LED flash
        SKIP:
        CLR C
        MOV A, COUNT               ;count--
        SUBB A, #1
        MOV COUNT, A
        MOV A, COUNT+1
        SUBB A, #0
        MOV COUNT+1, A
        POP PSW
        POP ACC
        RETI

;-----------------------------

END
Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload. Overflow from TL0 not only set TF0, but also reload TL0 with the content of TH0, which is preset by software. The reload leaves TH0 unchanged.

STC12C5A60S2 is able to generate a programmable clock output on P3.4. When T0CLKO bit in WAKE_CLKO SFR is set, T0 timer overflow pulse will toggle P3.4 latch to generate a 50% duty clock. The frequency of clock-out is as following:

\[
\begin{align*}
\frac{(\text{SYSclk})}{2} & \div \frac{256 - \text{TH0}}{256 - \text{TH0}} , & \text{when } T0x12=1 \\
\text{or} \quad \frac{(\text{SYSclk})}{12} & \div \frac{256 - \text{TH0}}{256 - \text{TH0}} , & \text{when } T0x12=0
\end{align*}
\]

**Example:** write a program using Timer 0 to create a 5KHz square wave on P1.0.

*Assembly Language Solution:*

```
ORG 0030H
MOV TMOD, #20H ;8-bit auto-reload mode
MOV TL0, #9CH ;initialize TL0
MOV TH0, #9CH ;-100 reload value in TH0
SETB TR0 ;Start Timer 0

LOOP: JNB TF0, LOOP ;Wait for overflow
       CLR TF0 ;Clear Timer overflow flag
       CPL P1.0 ;Toggle port bit
       SJMP LOOP ;Repeat

END
```
C Language Solution using Timer Interrupt:

```c
#include <REG51.H>  /* SFR declarations */
sbit portbit = P1^0;  /* Use variable portbit to refer to P1.0 */
main( )
{
    TMOD = 0x02;  /* timer 0, mode 2 */
    TH0 = 9CH;  /* 100us delay */
    TR0 = 1;  /* Start timer */
    IE = 0x82  /* Enable timer 0 interrupt */
    while(1);   /* repeat forever */
}

void T0ISR(void) interrupt 1
{
    portbit = !portbit;  /* toggle port bit P1.0 */
}
```

The following programs demonstrate Program Clock Output on Timer 0 pin when Timer 0 operates as 8-bit auto-reload Timer/Counter.

**C Program:**

```c
/* STC MCU International Limited */
/* STC 1T Series Programmable Clock Output Demo */
/* Mobile: (86)13922805190 */
/* Fax: 86-755-82944243 */
/* Tel: 86-755-82948412 */
/* Web: www.STCMCU.com */
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/* */
#include "reg51.h"

//define constants
#define FOSC 18432000L
#ifndef MODE1T
#define F38_4KHz (256-FOSC/2/38400)  //38.4KHz frequency calculation method of 1T mode
#else
#define F38_4KHz (256-FOSC/2/12/38400) //38.4KHz frequency calculation method of 12T mode
#endif

#define AUXR 0x8e  //Auxiliary register
#define WAKE_CLKO 0x8f  //wakeup and clock output control register
#define T0CLKO P3^4  //timer0 clock output pin
```

The following programs demonstrate Program Clock Output on Timer 0 pin when Timer 0 operates as 8-bit auto-reload Timer/Counter.
Assembly Program:

`;-----------------------------------------------------------------------------`
`; * main program */
void main()
{
#ifdef MODE1T
    AUXR = 0x80; // timer0 work in 1T mode
#endif
TMOD = 0x02; // set timer0 as mode2 (8-bit auto-reload)
TL0 = F38_4KHz; // initial timer0
TH0 = F38_4KHz; // initial timer0
TR0 = 1; // timer0 start running
WAKE_CLKO = 0x01; // enable timer0 clock output

while (1); // loop
}

#define MODE1T
#define MODE1T
ifdef MODE1T
F38_4KHz EQU 010H ; 38.4KHz frequency calculation method of 1T mode is (256-18432000/2/38400)
#else
F38_4KHz EQU 0ECH ; 38.4KHz frequency calculation method of 12T mode (256-18432000/2/12/38400)
#endif

; /* define SFR */
AUXR DATA 08EH ; Auxiliary register
WAKE_CLKO DATA 08FH ; wakeup and clock output control register
T0CLKO BIT P3.4 ; timer0 clock output pin

;-----------------------------------------------------------------------------

ORG 0000H
LJMP MAIN
; /************************************************************************
; main program */
MAIN:  
  #ifdef MODE1T
  MOV AUXR, #80H                ; timer0 work in 1T mode
  #endif
  MOV TMOD, #02H                ; set timer0 as mode2 (8-bit auto-reload)
  MOV TL0, #F38_4KHz            ; initial timer0
  MOV TH0, #F38_4KHz            ; initial timer0
  SETB TR0
  MOV WAKE_CLKO, #01H           ; enable timer0 clock output
  SJMP $                          

;*************************************************************************/

END
Mode 3

Timer 1 in Mode 3 simply holds its count, the effect is the same as setting TR1 = 0. Timer 0 in Mode 3 established TL0 and TH0 as two separate 8-bit counters. TL0 use the Timer 0 control bits: C/T, GATE, TR0, INT0 and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

![Timer/Counter 0 Mode 3: Two 8-Bit Counters](image-url)

<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/T=0</td>
<td>Timer 0 (8 bit)</td>
</tr>
<tr>
<td>C/T=1</td>
<td>Timer 1 (8 bits)</td>
</tr>
<tr>
<td>TR0</td>
<td>Interrupt</td>
</tr>
<tr>
<td>INT0</td>
<td>AUXR.7/T0x12=0</td>
</tr>
<tr>
<td>AUXR.7/T0x12=0</td>
<td>SYSelk</td>
</tr>
<tr>
<td>AUXR.7/T0x12=1</td>
<td>T0 Pin</td>
</tr>
<tr>
<td>SYSclk</td>
<td>AUXR.7/T0x12=0</td>
</tr>
<tr>
<td>AUXR.7/T0x12=1</td>
<td>SYSelk</td>
</tr>
<tr>
<td>TR1</td>
<td>Interrupt</td>
</tr>
<tr>
<td>TF0</td>
<td>Interrupt</td>
</tr>
<tr>
<td>TF1</td>
<td>Interrupt</td>
</tr>
</tbody>
</table>

Timer 1 in Mode 3 simply holds its count, the effect is the same as setting TR1 = 0. Timer 0 in Mode 3 established TL0 and TH0 as two separate 8-bit counters. TL0 use the Timer 0 control bits: C/T, GATE, TR0, INT0 and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 from Timer 1. Thus, TH0 now controls the “Timer 1” interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

![Timer/Counter 0 Mode 3: Two 8-Bit Counters](image-url)
7.2 Timer/Counter 1 Mode of Operation

Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF1. The counted input is enabled to the timer when TR1 = 1 and either GATE=0 or INT1 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT1, to facilitate pulse width measurements.) TR1 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 13-Bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ignored. Setting the run flag (TR1) does not clear the registers.

Mode 1

In this mode, the timer register is configured as a 16-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF1. The counted input is enabled to the timer when TR1 = 1 and either GATE=0 or INT1 = 1. (Setting GATE = 1 allows the Timer to be controlled by external input INT1, to facilitate pulse width measurements.) TR1 is a control bit in the Special Function Register TCON. GATE is in TMOD.

The 16-Bit register consists of all 8 bits of TH1 and the lower 8 bits of TL1. Setting the run flag (TR1) does not clear the registers.

Mode 1 is the same as Mode 0, except that the timer register is being run with all 16 bits.
**Example**: write a program using Timer 1 to create a 500Hz square wave on P1.0.

**Assembly Language Solution**:

```assembly
ORG 0030H
MOV TMOD, #10H ; 16-bit timer mode
MOV TH1, #0F8H ; -1000 (high byte)
MOV TL1, #30H ; -1000 (low byte)
SETB TR1 ; Start Timer 1

LOOP: JNB TF1, LOOP ; Wait for overflow
CLR TF1 ; Clear Timer overflow flag
CPL P1.0 ; Toggle port bit
SJMP LOOP ; Repeat

END
```

**C Language Solution**:

```c
#include <REG51.H> /* SFR declarations */
sbit portbit = P1^0; /* Use variable portbit to refer to P1.0 */

main( )
{
    TMOD = 0x10; /* timer 1, mode 1, 16-bit timer mode */
    while (1) /* repeat forever */
    {
        TH1 = 0xF8; /* -1000 (high byte) */
        TL1 = 0x30; /* -1000 (low byte) */
        TR1 = 1; /* Start timer 1 */
        while (TF0 !=1); /* wait for overflow */
        TR1 = 0; /* stop timer 1 */
        TF0 = 0; /* clear timer overflow flag */
        portbit = !(portbit); /* toggle P1.0 */
    }
}
```

There are another two simple programs that demostrates Timer 1 as 16-bit Timer/Counter, one written in C language while other in Assembly language.

**C Program**:

```c
/*-------------------------------------------------------------------------------*/
/* --- STC MCU International Limited ----------------------------------------*/
/* --- STC 1T Series 16-bit Timer Demo -------------------------------------*/
/* --- Mobile: (86)13922805190 ---------------------------------------------*/
/* --- Fax: 86-755-82944243 -----------------------------------------------*/
/* --- Tel: 86-755-82948412 -----------------------------------------------*/
/* --- Web: www.STCMCU.com -----------------------------------------------*/
/* If you want to use the program or the program referenced in the article, please specify in which data and procedures from STC */
/*-------------------------------------------------------------------------------*/
#include "reg51.h"

typedef unsigned char BYTE;
typedef unsigned int WORD;
```
/* define constants */
#define FOSC 18432000L  //Timer clock mode, comment this line is 12T mode, uncomment is 1T mode
#define MODE1T
#ifdef MODE1T
#define T1MS (65536-FOSC/1000)  //1ms timer calculation method in 1T mode
#else
#define T1MS (65536-FOSC/12/1000)  //1ms timer calculation method in 12T mode
#endif

/* define SFR */
sfr AUXR = 0x8e;  //Auxiliary register
sbit TEST_LED = P0^0;  //work LED, flash once per second

/* define variables */
WORD count;  //1000 times counter

/* Timer0 interrupt routine */
void tm1_isr() interrupt 3 using 1
{
    TL1 = T1MS;  //reload timer1 low byte
    TH1 = T1MS >> 8;  //reload timer1 high byte
    if (count-- == 0)  //1ms * 1000 -> 1s
    {
        count = 1000;  //reset counter
        TEST_LED = ! TEST_LED;  //work LED flash
    }
}

/* main program */
void main()
{
#ifdef MODE1T
    AUXR = 0x40;  //timer1 work in 1T mode
#endif
    TMOD = 0x10;  //set timer1 as mode1 (16-bit)
    TL1 = T1MS;  //initial timer1 low byte
    TH1 = T1MS >> 8;  //initial timer1 high byte
    TR1 = 1;  //timer1 start running
    ET1 = 1;  //enable timer1 interrupt
    EA = 1;  //open global interrupt switch
    count = 0;  //initial counter

    while (1);  //loop
Assembly Program:

;---------------------------------------------------------------------------------
;/* --- STC MCU International Limited ------------------------------------*/
;/* --- STC 1T Series 16-bit Timer Demo ----------------------------------*/
;/* --- Mobile: (86)13922805190 -------------------------------------------*/
;/* --- Fax: 86-755-82944243 -----------------------------------------------*/
;/* --- Tel: 86-755-82948412 -----------------------------------------------*/
;/* --- Web: www.STCMCU.com ---------------------------------------------*/
;/* If you want to use the program or the program referenced in the */
;/* article, please specify in which data and procedures from STC */
;/*----------------------------------------------------------------------------------*/

;/* define constants */
define MODE1T ;Timer clock mode, comment this line is 12T mode, uncomment is 1T mode

ifdef MODE1T
T1MS EQU 0B800H ;1ms timer calculation method in 1T mode is (65536-18432000/1000)
#else
T1MS EQU 0FA00H ;1ms timer calculation method in 12T mode is (65536-18432000/12/1000)
#endif

;/* define SFR */
AUXR DATA 8EH ;Auxiliary register
TEST_LED BIT P1.0 ;work LED, flash once per second

;/* define variables */
COUNT DATA 20H ;1000 times counter (2 bytes)

;-----------------------------------------------
ORG 0000H
LJMP MAIN

ORG 001BH
LJMP TM1_ISR

;-----------------------------------------------
;/* main program */
MAIN:
#ifdef MODE1T
MOV AUXR, #40H ;timer1 work in 1T mode
#else
MOV TMOD, #10H ;set timer1 as mode1 (16-bit)
MOV TL1, #LOW T1MS ;initial timer1 low byte
MOV TH1, #HIGH T1MS ;initial timer1 high byte
SETB TR1 ;timer1 start running
SETB ET1 ;enable timer1 interrupt
SETB EA ;open global interrupt switch
CLR A
MOV COUNT, A
MOV COUNT+1,A ;initial counter
#endif
SJMP $
;/* Timer1 interrupt routine */
TM1_ISR:
    PUSH ACC
    PUSH PSW
    MOV TL1, #LOW T1MS ;reload timer1 low byte
    MOV TH1, #HIGH T1MS ;reload timer1 high byte
    MOV A, COUNT
    ORL A, COUNT+1 ;check whether count(2byte) is equal to 0
    JNZ SKIP
    MOV COUNT, #LOW 1000 ;1ms * 1000 -> 1s
    MOV COUNT+1, #HIGH 1000
    CPL TEST_LED ;work LED flash
SKIP:
    CLR C
    MOV A, COUNT ;count--
    SUBB A, #1
    MOV COUNT, A
    MOV A, COUNT+1
    SUBB A, #0
    MOV COUNT+1, A
    POP PSW
    POP ACC
    RETI
END
Mode 2
Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reload. Overflow from TL1 not only set TFx, but also reload TL1 with the content of TH1, which is preset by software. The reload leaves TH1 unchanged.

STC12C5A60S2 is able to generate a programmable clock output on P3.5. When T1CLKO bit in WAKE_CLKO SFR is set, T1 timer overflow pulse will toggle P3.5 latch to generate a 50% duty clock. The frequency of clock-out is as following:

\[
\begin{align*}
(\text{SYSclk}/2) / (256 - \text{TH1}), & \quad \text{when } T1x12=1 \\
\text{or} \quad (\text{SYSclk}/2/12) / (256 - \text{TH1}), & \quad \text{when } T1x12=0
\end{align*}
\]

The following programs demonstrate Program Clock Output on Timer 1 pin when Timer 1 operates as 8-bit auto-reload Timer/Counter.

**C Program:**

```c
#include "reg51.h"

#include "reg51.h"

// define constants
#define FOSC 18432000L
//#define MODE1T                      //Timer clock mode, comment this line is 12T mode, uncomment is 1T mode
#ifndef MODE1T
#define F38_4KHz (256 - FOSC/2/38400)     //38.4KHz frequency calculation method of 1T mode
#else
#define F38_4KHz (256 - FOSC/2/12/38400)  //38.4KHz frequency calculation method of 12T mode
#endif
```

The following programs demonstrate Program Clock Output on Timer 1 pin when Timer 1 operates as 8-bit auto-reload Timer/Counter.
/* define SFR */
sfr AUXR = 0x8e; //Auxiliary register
sfr WAKE_CLKO = 0x8f; //wakeup and clock output control register
sbit T1CLKO = P3^5; //timer1 clock output pin

/* main program */
void main()
{
    #ifdef MODE1T
        AUXR = 0x40; //timer1 work in 1T mode
    #endif
    TMOD = 0x20; //set timer1 as mode2 (8-bit auto-reload)
    TL1 = F38_4KHz; //initial timer1
    TH1 = F38_4KHz; //initial timer1
    TR1 = 1; //timer1 start running
    WAKE_CLKO = 0x02; //enable timer1 clock output
    while (1); //loop
}

Assembly Program:
;/*---------------------------------------------------------------------------------*/
;/* --- STC MCU International Limited ------------------------------------*/
;/* --- STC 1T Series Programmable Clock Output Demo --------------*/
;/* --- Mobile: (86)13922805190 -------------------------------------------*/
;/* --- Fax: 86-755-82944243 -----------------------------------------------*/
;/* --- Tel: 86-755-82948412 ------------------------------------------------*/
;/* --- Web: www.STCMCU.com ------------------------------------------*/
;/* If you want to use the program or the program referenced in the */
;/* article, please specify in which data and procedures from STC */
;/*------------------------------------------------------------------------*/

; /* define constants */
#define MODE1T  ;Timer clock mode, comment this line in 12T mode, uncomment is 1T mode

#ifdef MODE1T
    F38_4KHz EQU 010H  ;38.4KHz frequency calculation method of 1T mode is (256-18432000/2/38400)
#else
    F38_4KHz EQU 0ECH  ;38.4KHz frequency calculation method of 12T mode (256-18432000/2/12/38400)
#endif

; /* define SFR */
AUXR DATA 08EH  ;Auxiliary register
WAKE_CLKO DATA 08FH  ;wakeup and clock output control register
T1CLKO BIT P3.5  ;timer1 clock output pin

STC MCU Limited. website: www.STCMCU.com
;------------------------------------------------------------------------

ORG    0000H
LJMP   MAIN

;------------------------------------------------------------------------

;/* main program */
MAIN:
#ifdef MODE1T
    MOV    AUXR, #40H ; timer1 work in 1T mode
#endif
    MOV    TMOD, #20H ; set timer1 as mode2 (8-bit auto-reload)
    MOV    TL1, #F38_4KHz ; initial timer1
    MOV    TH1, #F38_4KHz ; initial timer1
    SETB   TR1
    MOV    WAKE_CLKO, #02H ; enable timer1 clock output

    SJMP   $ ;------------------------------------------------------------------------

END
STC12C5A60S2 is able to generate a programmable clock output on P1.0. When BRTCLKO bit in WAKE_CLKO is set, BRT timer overflow pulse will toggle P1.0 latch to generate a 50% duty clock. The frequency of clock-out is as following:

\[
\text{(SYSclk/2) / (256 – BRT), \quad \text{when BRTx12=1}}
\]

or

\[
\text{(SYSclk/2/12) / (256 – BRT), \quad \text{when BRTx12=0}}
\]

The following program is an assembly language code that demonstrates timer 1 of STC12C5A60S2 series MCU acted as baud rate generator.

```assembly
;Declare STC11/10xx series MCU SFR
AUXR EQU 8EH

;Define baud rate auto-reload counter
;*************************************************************************
;The following Reload-Count and Baud is based on SYSclk =22.1184MHz, 1T mode, SMOD=1
;RELOAD_COUNT EQU 0FFH ;Baud=1,382,400 bps
;RELOAD_COUNT EQU 0FEH ;Baud=691,200 bps
;RELOAD_COUNT EQU 0FDH ;Baud=460,800 bps
;RELOAD_COUNT EQU 0FCH ;Baud=345,600 bps
;RELOAD_COUNT EQU 0FBH ;Baud=276,480 bps
;RELOAD_COUNT EQU 0FAH ;Baud=230,400 bps
;RELOAD_COUNT EQU 0F4H ;Baud=115,200 bps
;RELOAD_COUNT EQU 0E8H ;Baud=57,600 bps
;RELOAD_COUNT EQU 0DCH ;Baud=38,400 bps
;RELOAD_COUNT EQU 0B8H ;Baud=19,200 bps
;RELOAD_COUNT EQU 70H ;Baud=9,600 bps
```
The following Reload-Count and Baud is based on SYSclk = 1.8432MHz, 1T mode, SMOD=1

; RELOAD_COUNT  EQU  0FFH  ; Baud=115,200 bps
; RELOAD_COUNT  EQU  0FEH  ; Baud=57,600 bps
; RELOAD_COUNT  EQU  0FDH  ; Baud=38,400 bps
; RELOAD_COUNT  EQU  0FCH  ; Baud=28,800 bps
; RELOAD_COUNT  EQU  0FAH  ; Baud=19,200 bps
; RELOAD_COUNT  EQU  0F4H  ; Baud=9,600 bps
; RELOAD_COUNT  EQU  0E8H  ; Baud=4,800 bps
; RELOAD_COUNT  EQU  0D0H  ; Baud=2,400 bps
; RELOAD_COUNT  EQU  0A0H  ; Baud=1,200 bps

The following Reload-Count and Baud is based on SYSclk = 18.432MHz, 1T mode, SMOD=1

; RELOAD_COUNT  EQU  0FFH  ; Baud=1,152,000 bps
; RELOAD_COUNT  EQU  0FEH  ; Baud=576,000 bps
; RELOAD_COUNT  EQU  0FDH  ; Baud=288,000 bps
; RELOAD_COUNT  EQU  0FCH  ; Baud=144,000 bps
; RELOAD_COUNT  EQU  0F6H  ; Baud=115,200 bps
; RELOAD_COUNT  EQU  0ECH  ; Baud=57,600 bps
; RELOAD_COUNT  EQU  0E2H  ; Baud=38,400 bps
; RELOAD_COUNT  EQU  0D8H  ; Baud=28,800 bps
; RELOAD_COUNT  EQU  0C4H  ; Baud=19,200 bps
; RELOAD_COUNT  EQU  088H  ; Baud=9,600 bps

The following Reload-Count and Baud is based on SYSclk = 18.432MHz, 12T mode, SMOD=0

; RELOAD_COUNT  EQU  0FBH  ; Baud=9,600 bps
; RELOAD_COUNT  EQU  0F6H  ; Baud=4,800 bps
; RELOAD_COUNT  EQU  0ECH  ; Baud=2,400 bps
; RELOAD_COUNT  EQU  0D8H  ; Baud=1,200 bps

The following Reload-Count and Baud is based on SYSclk = 18.432MHz, 12T mode, SMOD=1

; RELOAD_COUNT  EQU  0FBH  ; Baud=9,600 bps
; RELOAD_COUNT  EQU  0F6H  ; Baud=4,800 bps
; RELOAD_COUNT  EQU  0ECH  ; Baud=2,400 bps
; RELOAD_COUNT  EQU  0D8H  ; Baud=1,200 bps
RELOAD_COUNT EQU 0FFH  ;Baud=28,800 bps
RELOAD_COUNT EQU 0FEH  ;Baud=14,400 bps
RELOAD_COUNT EQU 0FDH  ;Baud=9,600 bps
RELOAD_COUNT EQU 0FAH  ;Baud=4,800 bps
RELOAD_COUNT EQU 0F4H  ;Baud=2,400 bps
RELOAD_COUNT EQU 0E8H  ;Baud=1,200 bps

RELOAD_COUNT EQU 0FFH  ;Baud=57,600 bps
RELOAD_COUNT EQU 0FEH  ;Baud=28,800 bps
RELOAD_COUNT EQU 0FDH  ;Baud=14,400 bps
RELOAD_COUNT EQU 0FAH  ;Baud=9,600 bps
RELOAD_COUNT EQU 0F4H  ;Baud=4,800 bps
RELOAD_COUNT EQU 0D0H  ;Baud=1,200 bps

LED_MCU_START EQU P1.7 ;MCU operating LED indicator

ORG 0000H
AJMP MAIN

ORG 0023H
AJMP UART_Interrupt ;Jump into RS232 UART-Interrupt service subroutine
NOP
NOP

MAIN:
MOV SP, #7FH ;Set stack pointer
CLR LED_MCU_START ;Open MCU operating LED indicator
ACALL Initial_UART ;Initialize UART
MOV R0, #30H ;30H = the ASCII code of printable character '0'
MOV R2, #10 ;Send ten characters '0123456789'

LOOP:
MOV A, R0
ACALL Send_One_Byte ;Send one byte
;if Character-Display, display '0123456789'
;if Hexadecimal-Display, display '30 31 32 33 34 35 36 37 38 39'
INC R0
DJNZ R2, LOOP

MAIN_WAIT:
SJMP MAIN_WAIT ;infinite circle

;******************************************************************************
UART_Interrupt: ;UART-Interrupt service subroutine
    JB RI, Is_UART_Receive ;Clear serial port transmit interrupt flag
    CLR TI
    RETI

Is_UART_Receive:
    CLR RI
    PUSH ACC
    MOV A, SBUF ;acquire the received byte
    ACALL Send_One_Byte ;re-send the received byte
    POP ACC
    RETI

;-----------------------------------------------------------------------------------------------------------------------

Initial_UART: ;Initialize UART
;SCON Bit: 7 6 5 4 3 2 1 0
;   SM0/FE SM1 SM2 REN TB8 RB8 TI RI
MOV SCON, #50H ;0101,0000  8-bit variable baud rate,no odd parity bit
MOV TMOD, #21H ;Use Timer 1 as 8 bit auto-reload counter
MOV TH1, #RELOAD_COUNT ;Set auto-reload count of Timer 1
MOV TL1, #RELOAD_COUNT

;----------------------------------------------------------------------------------------------------------------------
;  ORL  PCON, #80H   ;baud rate double
;----------------------------------------------------------------------------------------------------------------------
;  ORL  AUXR, #01000000B  ;Use Timer 1 in 1T mode
ANL AUXR, #10111111B ;Use Timer 1 in 12T mode

;----------------------------------------------------------------------------------------------------------------------
SETB R1 ; Start up Timer 1
SETB ES
SETB EA
RET

;-----------------------------------------------------------------------------------------------------------------------

;Portal parameter: A= the byte to send
Send_One_Byte: ;Send one byte
    CLR ES
    CLR TI ;Clear serial port transmit interrupt flag
    MOV SBUF, A

Wait_Send_Finish:
    JNB TI, Wait_Send_Finish ;Wait to finish send
    CLR TI
    SETB ES
    RET

;-------------------------------------------------------------------------------------------------------------------------

END
The example program that demonstrates programmable clock out as follows:

/* SYSclk = 18.432MHz; T0,T1 and independent baud rate generator all in 1T mode. */
#include "reg51.h"

sfr WAKE_CLKO = 0x8F;
sfr AUXR = 0x8E;
sfr BRT = 0x9C;

main ( )
{
    TMOD = 0x22;
    // T0 and T1 all in mode 2, 8-bit auto-reload counter
    AUXR = (AUXR | 0x80);  // T0 in 1T mode
    AUXR = (AUXR | 0x40);  // T1 in 1T mode
    AUXR = (AUXR | 0x04);  // Independent Baud Rate Generator in 1T mode

    BRT = (256-74);   //8-bit reload value in BRT, SYSclkO is 124.540KHz
    TH0 = (256-74);   //8-bit reload value in TH0, SYSclkO=18432000/2/74=124540.54
    TH1 = (256-240);   //8-bit reload value in TH1, SYSclkO=18432000/2/240=38400
    WAKE_CLKO = ( WAKE_CLKO | 0x07);    //allow T0, T1 and Independent Baud rate Generator output clock
    TR0 = 1;   //start timer 0 as counter, system clock is divided and output
    TR1 = 1;   //start timer 1 as counter, system clock is divided and output
    AUXR = (AUXR | 0x10); //start independent baud rate generator as counter
    //system clock has been output and could be watched through oscilloscope
    while(1);
}
C Program:

/*---------------------------------------------*
/* --- STC MCU International Limited          */
/* --- STC 1T Series Programmable Clock Output Demo */
/* --- Mobile: (86)13922805190 ------------------------*/
/* --- Fax: 86-755-82944243 ------------------------*/
/* --- Tel: 86-755-82948412 ------------------------*/
/* --- Web: www.STCMCU.com ----------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*---------------------------------------------*/

#include "reg51.h"

//---------------------------------------------------------------------------------------------------------------
/* define constants */
#define FOSC 18432000L
#ifndef MODE1T
    #define F38_4KHz (256-FOSC/2/38400)     //38.4KHz frequency calculation method of 1T mode
#else
    #define F38_4KHz (256-FOSC/2/12/38400) //38.4KHz frequency calculation method of 12T mode
#endif

//---------------------------------------------------------------------------------------------------------------
/* define SFR */
sfr AUXR       =  0x8e;                 //Auxiliary register
sfr WAKE_CLKO =  0x8f;                //wakeup and clock output control register
sfr BRT        =  0x9c;
sbit BRTCLKO =  P1^0;                 //BRT clock output pin

//---------------------------------------------------------------------------------------------------------------
/* main program */
void main()
{
#ifndef MODE1T
    AUXR = 0x04;                      //BRT work in 1T mode
#endif
    BRT = F38_4KHz;                   //initial BRT
    AUXR |= 0x10;                     //BRT start running
    WAKE_CLKO = 0x04;                //enable BRT clock output

    while (1);                        //loop
}
Assembly Program:

;-----------------------------------------------
ORG 0000H
LJMP MAIN
;-----------------------------------------------

/* define constants */
define MODE1T ;Timer clock mode, comment this line is 12T mode, uncomment is 1T mode

#ifdef MODE1T
F38_4KHz EQU 010H ;38.4KHz frequency calculation method of 1T mode is (256-18432000/2/38400)
#else
F38_4KHz EQU 0ECH ;38.4KHz frequency calculation method of 12T mode (256-18432000/2/12/38400)
#endif

;-----------------------------------------------
; define SFR */
AUXR DATA 08EH ;Auxiliary register
WAKE_CLKO DATA 08FH ;wakeup and clock output control register
BRT DATA 09CH
BRTCLKO BIT P1.0 ;BRT clock output pin

;-----------------------------------------------

ORG 0000H
LJMP MAIN

;-----------------------------------------------

/* main program */
MAIN:
#ifdef MODE1T
MOV AUXR, #04H ;BRT work in 1T mode
#endif
MOV BRT, #F38_4KHz ;initial BRT reload value
ORL AUXR, #10H ;BRT start run
MOV WAKE_CLKO, #04H ;enable BRT clock output

SJMP $

;-----------------------------------------------

END
Application note for Timer in practice:

(1) Real-time Timer
Timer/Counter start running, When the Timer/Counter is overflow, the interrupt request generated, this action handle by the hardware automatically, however, the process which from propose interrupt request to respond interrupt request requires a certain amount of time, and that the delay interrupt request on-site with the environment varies, it normally takes three machine cycles of delay, which will bring real-time processing bias. In most occasions, this error can be ignored, but for some real-time processing applications, which require compensation.

Such as the interrupt response delay, for timer mode 0 and mode 1, there are two meanings: the first, because of the interrupt response time delay of real-time processing error; the second, if you require multiple consecutive timing, due to interruption response delay, resulting in the interrupt service program once again sets the count value is delayed by several count cycle.

If you choose to use Timer/Counter mode 1 to set the system clock, these reasons will produce real-time error for this situation, you should use dynamic compensation approach to reducing error in the system clock, compensation method can refer to the following example program.

```
CLR EA ;disable interrupt
MOV A, TLx ;read TLx
ADD A, #LOW ;LOW is low byte of compensation value
MOV TLx, A ;update TLx
MOV A, THx ;read THx
ADDC A, #HIGH ;HIGH is high byte of compensation value
MOV THx, A ;update THx
SETB EA ;enable interrupt
```

(2) Dynamic read counts
When dynamic read running timer count value, if you do not pay attention to could be wrong, this is because it is not possible at the same time read the value of the TLx and THx. For example the first reading TLx then THx, because the timer is running, after reading TLx, TLx carry on the THx produced, resulting in error; Similarly, after the first reading of THx then TLx, also have the same problems.

A kind of way avoid reading wrong is first reading THx then TLx and read THx once more, if the THx twice to read the same value, then the read value is correct, otherwise repeat the above process. Realization method reference to the following example code.

```
RDTM: MOV A, THx ;save THx to ACC
MOV R0, TLx ;save TLx to R0
CJNE A, THx, RDTM ;read THx again and compare with the previous value
MOV R1, A ;save THx to R1
```

Chapter 8. Serial Interface (UART)

8.1 UART with enhanced function

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. (However, if the first byte still hasn’t been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit share the same SFR – SBUF, but actually there are two SBUF in the chip, one is for transmit and the other is for receive.

The serial port (UART) can be operated in 4 different modes: Mode 0 provides synchronous communication while Modes 1, 2, and 3 provide asynchronous communication. The asynchronous communication operates as a full-duplex Universal Asynchronous Receiver and Transmitter (UART), which can transmit and receive simultaneously and at different baud rates.

Serial communication involves the transmission of bits of data through only one communication line. The data are transmitted bit by bit in either synchronous or asynchronous format. Synchronous serial communication transmits one whole block of characters in synchronization with a reference clock while asynchronous serial communication randomly transmits one character at any time, independent of any clock.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Bit Address and Symbol</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRT</td>
<td>Baud-Rate Timer</td>
<td>9CH</td>
<td>0000 0000B</td>
<td></td>
</tr>
<tr>
<td>AUXR</td>
<td>Auxiliary register</td>
<td>8EH</td>
<td>T0x12</td>
<td>T1x12</td>
</tr>
<tr>
<td>SCON</td>
<td>Serial Control</td>
<td>98H</td>
<td>SM0/FE</td>
<td>SM1</td>
</tr>
<tr>
<td>SBUF</td>
<td>Serial Buffer</td>
<td>99H</td>
<td>xxxx xxxxB</td>
<td></td>
</tr>
<tr>
<td>PCON</td>
<td>Power Control</td>
<td>87H</td>
<td>SMOD</td>
<td>SMOD0</td>
</tr>
<tr>
<td>IE</td>
<td>Interrupt Enable</td>
<td>A8H</td>
<td>EA</td>
<td>ELVD</td>
</tr>
<tr>
<td>IP</td>
<td>Interrupt Priority Low</td>
<td>B8H</td>
<td>PPCA</td>
<td>PLVD</td>
</tr>
<tr>
<td>IPH</td>
<td>Interrupt Priority High</td>
<td>B7H</td>
<td>PPCAH</td>
<td>PLVDH</td>
</tr>
<tr>
<td>SADEN</td>
<td>Slave Address Mask</td>
<td>B9H</td>
<td>0000 0000B</td>
<td></td>
</tr>
<tr>
<td>SADDR</td>
<td>Slave Address</td>
<td>A9H</td>
<td>0000 0000B</td>
<td></td>
</tr>
<tr>
<td>S2CON</td>
<td>S2 Control</td>
<td>9AH</td>
<td>S2SM0</td>
<td>S2SM1</td>
</tr>
<tr>
<td>S2SBUF</td>
<td>S2 Serial Buffer</td>
<td>9BH</td>
<td>xxxx xxxxB</td>
<td></td>
</tr>
<tr>
<td>AUXR1</td>
<td>Auxiliary register1</td>
<td>A2H</td>
<td>-</td>
<td>PCA_P4</td>
</tr>
<tr>
<td>IE2</td>
<td>Interrupt Enable 2</td>
<td>AFH</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2</td>
<td>2rd Interrupt Priority Low register</td>
<td>B5H</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IP2H</td>
<td>2rd Interrupt Priority Low register</td>
<td>B6H</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>WAKE_CLKO</td>
<td>CLK_Output Power down Wake-up control register</td>
<td>8FH</td>
<td>PCAAWAKEUP</td>
<td>RXD_PIN_IE</td>
</tr>
</tbody>
</table>
### SCON register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SM0/FE</td>
<td>SM1</td>
<td>SM2</td>
<td>REN</td>
<td>TB8</td>
<td>RB8</td>
<td>TI</td>
<td>RI</td>
</tr>
</tbody>
</table>

FE: Framing Error bit. The SMOD0 bit must be set to enable access to the FE bit
- 0: The FE bit is not cleared by valid frames but should be cleared by software.
- 1: This bit set by the receiver when an invalid stop bit id detected.

SM0,SM1 : Serial Port Mode Bit 0/1.
- SM0 0: 8-bit shift register
- SM0 1: 8-bit UART
- SM1 0: 9-bit UART
- SM1 1: 9-bit UART

SM2 : Enable the automatic address recognition feature in mode 2 and 3. If SM2=1, RI will not be set unless the received 9th data bit is 1, indicating an address, and the received byte is a Given or Broadcast address. In mode1, if SM2=1 then RI will not be set unless a valid stop bit was received, and the received byte is a Given or Broadcast address. In mode 0, SM2 should be 0.

REN : When set enables serial reception.
TB8 : The 9th data bit which will be transmitted in mode 2 and 3.
RB8 : In mode 2 and 3, the received 9th data bit will go into this bit.
TI : Transmit interrupt flag.
RI : Receive interrupt flag.

### SBUF register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## BRT register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It is used as the reload register for generating the baud-rate of the secondary UART.

### PCON: Power Control register

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SMOD</td>
<td>SMOD0</td>
<td>LVDF</td>
<td>POF</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
<td>IDL</td>
</tr>
</tbody>
</table>

SMOD: double Baud rate control bit.
- 0 : Disable double Baud rate of the UART.
- 1 : Enable double Baud rate of the UART in mode 1,2,or 3.

SMOD0: Frame Error select.
- 0 : SCON.7 is SM0 function.
- 1 : SCON.7 is FE function. Note that FE will be set after a frame error regardless of the state of SMOD0.
AUXR register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
<td>S2SMOD</td>
<td>BRTx12</td>
<td>EXTRAM</td>
<td>S1BRS</td>
</tr>
</tbody>
</table>

T1x12
0 : The clock source of Timer 1 is SYSclk/12.
1 : The clock source of Timer 1 is SYSclk/1.

UART_M0x6 : Serial Port mode 0 baud rate selector.
0 : Clear to select SYSclk/12 as the baud rate for UART Mode 0.
1 : Set to select SYSclk/2 as the baud rate for UART Mode 0.

BRTR: Independent Baud-rate generator control bit.
0 : The independent baud-rate generator is stoped.
1 : The independent baud-rate generator is stoped.

S2SMOD
0 : Default.
1 : The baud-rate UART2(S2) is doubled.

BRTx12
0 : The independent baud-rate is incremented every 12 system clocks.
1 : The independent baud-rate is incremented every system clock.

S1BRS
0 : select Timer 1 as the baud-rate generator of the enhanced UART.
1 : Timer 1 is replaced by the independent baud-rate generator for use of the enhanced UART. In other word, time1 is released to use in other functions.

SADEN: Slave Address Mask register

SADDR: Slave Address register

SADDR register is combined with SADEN register to form Given/Broadcast Address for automatic address recognition. In fact, SADEN function as the "mask" register for SADDR register. The following is the example for it.

\[
\begin{align*}
\text{SADDR} & = 1100\ 0000 \\
\text{SADEN} & = 1111\ 1101 \\
\text{Given} & = 1100\ 0000 \\
\end{align*}
\]

The Given slave address will be checked except bit 1 is treated as "don't care".

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zero in this result is considered as "don't care" and a Broadcast Address of all "don't care". This disables the automatic address detection feature.

WAKE_CLKO register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>PCAWAKEUP</td>
<td>RXD_PIN_IE</td>
<td>T1_PIN_IE</td>
<td>T0_PIN_IE</td>
<td>LVD_WAKE</td>
<td>BRTCKLO</td>
<td>T1CKLO</td>
<td>T0CKLO</td>
</tr>
</tbody>
</table>

RXD_PIN_IE : When set and the associated-UART interrupt control registers is configured correctly, the RXD pin (P3.0) is enabled to wake up MCU from power-down state.

BRTCKLO : When set, P1.0 is enabled to be the clock output of Baud-Rate Timer (BRT). The clock rate is BRG overflow rate divided by 2.
8.1.1 UART Mode of Operation

8-Bit Shift Register (Mode 0)

Mode 0, selected by writing 0s into bits SM1 and SM0 of SCON, puts the serial port into 8-bit shift register mode. Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted/received with the least-significant (LSB) first. The baud rate is fixed at 1/12 the System clock cycle in the default state. If AUXR.5(UART_M0x6) is set, the baud rate is 1/2 System clock cycle.

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full system clock cycle will elapse between “write to SBUF,” and activation of SEND.

SEND transfers the output of the shift register to the alternate output function line of P3.0, and also transfers Shift Clock to the alternate output function line of P3.1. At the falling edge of the Shift Clock, the contents of the shift register are shifted one position to the right.

As data bits shift out to the right, “0” come in from the left. When the MSB of the data byte is at the output position of the shift register, then the “1” that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contains zeroes. This condition flags the TX Control block to do one last shift and then deactivate SEND and set TI. Both of these actions occur after "write to SBUF".

Reception is initiated by the condition REN=1 and RI=0. After that, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE. RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. At RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin the rising edge of Shift clock.

As data bits come in from the right, “1”s shift out to the left. When the “0” that was initially loaded into the right-most position arrives at the left-most position in the shift register, it flags the RX Control block to do one last shift and load SBUF. Then RECEIVE is cleared and RI is set.
STC MCU Limited.

www.STCMCU.com

Mobile:(86)13922805190  Tel:086-755-82948412  Fax:86-755-82944243

INTERNAL BUS

WRITE TO SBUF

SEND
SHIF
TXD(SHIFT CLOCK)
TXD(P3.1)
RXD(P3.0)

WRITE TO SCON(CLEAR RI)

RXD(DATA IN)
TXD(SHIFT CLOCK)

Serial Port Mode 0
8-Bit UART with Variable Baud Rate (Mode 1)

10 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits and a stop bit(1). One receive, the stop bit goes into RB8 in SFR – SCON. The baud rate is determined by the Timer 1 or BRT overflow rate.

\[
\text{Baud rate in mode 1} = \begin{cases} 
\frac{2^{\text{SMOD}}}{32} \times \text{timer 1 overflow rate} & \text{if AUXR.0/S1BRS=0} \\
\frac{2^{\text{SMOD}}}{32} \times \text{BRT overflow rate} & \text{if AUXR.0/S1BRS=1}
\end{cases}
\]

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads a “1” into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually happens at the next rollover of divided-by-16 counter. Thus the bit times are synchronized to the divided-by-16 counter, not to the “write to SBUF” signal.

The transmission begins with activation of SEND, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that.

As data bits shift out to the right, zeroes are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate SEND and set TI. This occurs at the 10th divide-by-16 rollover after “write to SBUF.”

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times the established baud rate. When a transition is detected, the divided-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divided-by-16 counter aligns its roll-overs with the boundaries of the incoming bit times.

The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not a 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the left most position in the shift register,(which is a 9-bit register in Mode 1), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI=0 and
2) Either SM2=0, or the received stop bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition in RXD.
Serial Port Mode 1

TXD

START BIT

STOP BIT

DATA

SHIFT

SEND

TRANSMIT

WRITE TO SBUF

RXD

START BIT

STOP BIT

BIT DETECTOR SAMPLE TIMES

SHIFT

RI

Serial Port Mode 1
9-Bit UART with Fixed Baud Rate (Mode 2)

11 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits, a programmable 9th data bit and a stop bit(1). On transmit, the 9th data bit comes from TB8 in SCON. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the System clock cycle.

\[
\text{Baud rate in mode 2} = \left(\frac{2^{\text{SMOD}}}{64}\right) \times \text{SYSclk}
\]

Transmission is initiated by any instruction that uses SBUF as a destination register. The “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually happens at the next rollover of divided-by-16 counter. Thus the bit times are synchronized to the divided-by-16 counter, not to the “write to SBUF” signal.

The transmission begins when /SEND is activated, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a ‘1’(the stop bit) into the 9th bit position on the shift register. Thereafter, only “0”s are clocked in. As data bits shift out to the right, “0”s are clocked in from the left. When TB8 of the data byte is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contains “0”s. This condition flags the TX Control unit to do one last shift, then deactivate /SEND and set TI. This occurs at the 11th divided-by-16 rollover after “write to SBUF”.

Reception is initiated by a 1-to-0 transition detected at RXD. For this purpose, RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divided-by-16 counter is immediately reset, and IFFH is written into the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done to reject noise. In order to reject false bits, if the value accepted during the first bit time is not a 0, the receive circuits are reset and the unit continues looking for another 1-to-0 transition. If the start bit is valid, it is shifted into the input shift register, and reception of the rest of the frame proceeds.

As data bits come in from the right, “1”s shift out to the left. When the start bit arrives at the leftmost position in the shift register,(which is a 9-bit register in Mode-2 and 3), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8 and to set RI is generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

1) RI=0 and
2) Either SM2=0, or the received 9th data bit = 1

If either of these two conditions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the first 8 data bits go into SBUF, and RI is activated. At this time, whether or not the above conditions are met, the unit continues looking for a 1-to-0 transition at the RXD input.

Note that the value of received stop bit is irrelevant to SBUF, RB8 or RI.
Serial Port Mode 2
9-Bit UART with Variable Baud Rate (Mode 3)

Mode 3 is the same as mode 2 except the baud rate is variable.

\[
\text{Baud rate in mode 3} = \begin{cases} 
(2^{\text{SMOD}}/32) \times \text{timer 1 overflow rate} & \text{(if AUXR.0/S1BRS=0)} \\
(2^{\text{SMOD}}/32) \times \text{BRT overflow rate} & \text{(if AUXR.0/S1BRS=1)} 
\end{cases}
\]

In all four modes, transmission is initiated by any instruction that use SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit with 1-to-0 transition if REN=1.

8.1.2 Frame Error Detection

When used for frame error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6(SMOD0). If SMOD0 is set then SCON.7 functions as FE, SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software. Refer to the following figure.

8.1.3 Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren’t being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.
8.1.4 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, Mode 2 and Mode 3, the Receive interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a “1” to indicate that the received information is an address and not data.

The 8-bit mode is called Mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the broadcast address. Two special function registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized which excluding others. The following examples will help to show the versatility of this scheme:

| Slave 0       | SADDR = 1100 0000 |
|              | SADEN = 1111 1101 |
|              | GIVEN = 1100 00x0  |
| Slave 1       | SADDR = 1100 0000 |
|              | SADEN = 1111 1110 |
|              | GIVEN = 1100 000x |

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a “0” in bit 0 and it ignores bit 1. Slave 1 requires a “0” in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 11000010 since slave 1 requires a “0” in bit 1. A unique address for slave 1 would be 11000001 since a “1” in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0=0 (for slave 0) and bit 1 =0 (for salve 1). Thus, both could be addressed with 1100000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

| Slave 0       | SADDR = 1100 0000 |
|              | SADEN = 1111 1001 |
|              | GIVEN = 1100 0xx0  |
| Slave 1       | SADDR = 1110 0000 |
|              | SADEN = 1111 1010 |
|              | GIVEN = 1110 0x0x  |
| Slave 2       | SADDR = 1110 0000 |
|              | SADEN = 1111 1100 |
|              | GIVEN = 1110 00xx  |
In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 11100110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 11100101. Slave 2 requires that bit 2 = 0 and its unique address is 11100011. To select Slave 0 and 1 and exclude Slave 2, use address 11100100, since it is necessary to make bit 2 = 1 to exclude Slave 2.

The Broadcast Address for each slave is created by taking the logic OR of SADDR and SADEN. Zeros in this result are treated as don’t cares. In most cases, interpreting the don’t cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR and SADEN are loaded with “0”s. This produces a given address of all “don’t cares as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

**Example:** write a program that continually transmits characters from a transmit buffer. If incoming characters are detected on the serial port, store them in the receive buffer starting at internal RAM location 50H. Assume that the STC12C5A60S2 series MCU serial port has already been initialized in mode 1.

**Solution:**

```asm
ORG 0030H
MOV R0, #30H   ;pointer for tx buffer
MOV R1, #50H   ;pointer for rx buffer
LOOP: JB RI, RECEIVE  ;character received?
        ;yes: process it
        JB TI, TX   ;previous character transmitted?
        ;yes: process it
        SJMP LOOP     ;no: continue checking
TX: MOV A, @R0    ;get character from tx buffer
    MOV C, P    ;put parity bit in C
    CPL C    ;change to odd parity
    MOV ACC.7, C   ;add to character code
    CLR TI    ;clear transmit flag
    MOV SBUF, A    ;send character
    CLR ACC.7    ;strip off parity
    INC R0    ;point to next character in buffer
    CJNE R0, #50H, LOOP   ;end of buffer?
        ;no: continue
    MOV R0, #30H   ;yes: recycle
    SJMP LOOP     ;continue checking
RX: CLR RI    ;clear receive flag
    MOV A, SBUF  ;read character into A
    MOV C, P    ;for odd parity in A, P should be set
    CPL C    ;complementing correctly indicates "error"
    CLR ACC.7    ;strip off parity
    MOV @R1, A    ;store received character in buffer
    INC R1    ;point to next location in buffer
    SJMP LOOP     ;continue checking
END
```
8.1.5 Baud Rates

The baud rate in Mode 0 is fixed:

\[
\text{Mode 0 Baud Rate} = \frac{\text{SYSclk}}{12} \quad \text{when AUXR.5/UART_M0x6 =0}
\]

or \[
\text{Mode 0 Baud Rate} = \frac{\text{SYSclk}}{2} \quad \text{when AUXR.5/UART_M0x6 =1}
\]

The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If \( \text{SMOD} = 0 \) (which is the value on reset), the baud rate \( \frac{1}{64} \) the System clock cycle. If \( \text{SMOD} = 1 \), the baud rate is \( \frac{1}{32} \) the System clock cycle.

\[
\text{Mode 2 Baud Rate} = \frac{2^\text{SMOD}}{64} \times (\text{SYSclk})
\]

In the STC12C5A60S2, the baud rates in Modes 1 and 3 are determined by Timer1 or BRT overflow rate. The baud rate in Mode 1 and 3 are fixed:

\[
\text{Mode 1,3 Baud rate} = \left( \frac{2^\text{SMOD}}{32} \right) \times \text{Timer 1 overflow rate} \quad \text{if AUXR.0/S1BRS=0}
\]

or \[
\text{Mode 1,3 Baud rate} = \left( \frac{2^\text{SMOD}}{32} \right) \times \text{BRT overflow rate} \quad \text{if AUXR.0/S1BRS=1}
\]

Timer 1 overflow rate = \( \frac{\text{SYSclk}/12}{(256 - TH1)} \),

BRT overflow rate = \( \frac{\text{SYSclk}/2}{(256 - \text{BRT})} \), \quad \text{when AUXR.2/BRTx12=1}

or \( \frac{\text{SYSclk}/12}{(256 - \text{BRT})} \), \quad \text{when AUXR.2/BRTx12=0}

When Timer 1 is used as the baud rate generator, the Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either “timer” or “comter” operation, and in any of its 3 running modes. In the most typical applications, it is configured for “timer” operation, in the auto-reload mode (high nibble of \( \text{TMOD} = 0010B \)).

One can achieve very low baud rate with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of \( \text{TMOD} = 0001B \)), and using the Timer 1 interrupt to do a 16-bit software reload.

The following figure lists various commonly used baud rates and how they can be obtained from Timer 1.

<table>
<thead>
<tr>
<th>Baud Rate</th>
<th>( f_{osc} )</th>
<th>SMOD</th>
<th>Timer 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode 0 MAX:1MHZ</td>
<td>12MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Mode 2 MAX:375K</td>
<td>12MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Mode 1,3:62.5K</td>
<td>12MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>19.2K</td>
<td>11.059MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>9.6K</td>
<td>11.059MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>4.8K</td>
<td>11.059MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2.4K</td>
<td>11.059MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1.2K</td>
<td>11.059MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>137.5</td>
<td>11.986MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>110</td>
<td>6MHZ</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>110</td>
<td>12MHZ</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Timer 1 Generated Commonly Used Baud Rates
The following program is an example that demonstrates UART communication with independent baud rate generator.

```c
#include<reg51.h>
#include<intrins.h>
sfr AUXR  = 0x8E;
sfr AUXR1 = 0xA2;
sfr BRT   = 0x9C;
sbit MCU_Start_LED = P1^4;
unsigned char array[9] = {0,2,4,6,8,10,12,14,16};
unsigned char array[9] = {0x00, 0x02, 0x04, 0x06, 0x08, 0x0A, 0x0C,0x0E, 0x10};
#define RELOAD_COUNT   0xfb //18.432MHz, 12T, SMOD=0, 9600bps

void serial_port_initial( );
void send_UART(unsigned char);
void UART_Interrupt_Receive(void);
void delay (void);
void display_MCU_Start_LED (void);

void main(void)
{
    unsigned char i = 0;
    serial_port_initial( ); //initialize serial port
    display_MCU_Start_LED( ); //open LED indicator, MCU start-up
    send_UART (0x34); //UART send data
    send_UART(0xa7);
    for(i=0; i<9; i++)
    {
        send_UART(array[i]);
    }
    while(1);
}
```
void serial_port_initial()   //use Timer 1 for baud rate generator
{
    SCON = 0x50;   //0101,0000   8-bit variable baud rate, no odd parity bit
    TMOD = 0x21;   //0011,0001   use Timer 1 for 8-bit auto-reload counter
    TH1  = RELOAD_COUNT; //set Timer 1 auto-reload value
    TL1 = RELOAD_COUNT;
    TR1 = 1;   //start Timer 1
    ES = 1;   //enable serial port interrupt
    EA = 1;   //set global enable bit
}
*/

void serial_port_initial()   //use independent baud rate generator for baud rate generator
{
    SCON = 0x50;   //0101,0000   8-bit variable baud rate, no odd parity bit
    BRT  = RELOAD_COUNT;
    AUXR = 0x11;
    //T0x12, T1x12, UART_M0x6, BRTR, BRTx12, XRAM, S1BRS
    //Baud = SYSclk / (256-RELOAD_COUNT)/32/12 (12T mode)
    //Baud = SYSclk / (256-RELOAD_COUNT)/32  (1T mode)
    //Baud = 1, start independent baud rate generator
    //S1BRS = 1, UART use independent baud rate generator for baud rate generator
    //Timer 1 can be released to timer, counter or clock-output
    //AUXR =0x80;  //if enable this instruction, serial port would be P1 port rather than P3
    ES = 1;   //enable serial port interrupt
    EA = 1;   //set global enable bit
}

void send_UART(unsigned char i)
{
    ES = 0;  //close serial port interrupt
    TI = 0;  //clear UART transmit interrupt flag
    SBUF = i;
    while (TI == 0);  //wait to finish transmit
    TI = 0;  //clear UART transmit interrupt flag
    ES = 1;   //enable serial port interrupt
}

void UART_Interrupt_Receive (void) interrupt 4
{
    unsigned char k = 0;
    if (RI == 1)
    {
        RI = 0;
        k = SBUF;
        send_UART (k+1);
    }
else
{
    TI = 0;
}
}

void delay (void)
{
    unsigned int j = 0;
    unsigned int g = 0;
    for (j=0; j<5; j++)
    {
        for (g=0; g<50000; g++)
        {
            _nop_( );
            _nop_( );
            _nop_( );
        }
    }
}

void display_MCU_Start_LED (void)
{
    unsigned char i = 0;
    for (i=0; i<5; i++)
    {
        MCU_Start_LED = 0;  //open MCU-Start-LED indicator
delay();
        MCU_Start_LED = 1;  //close MCU-Start-LED indicator
delay();
        MCU_Start_LED = 0;  //open MCU-Start-LED indicator
delay();
    }
}
8.2 Secondary UART (S2)

S2 is the secondary UART of STC12C5A60S2 that its function is fully the same with the major UART described in last section and only with the exception that no enhanced function included. An additional baud-rate generator (BRT) is available in S2 to simplify the baud-rate generation and release Timer1 for use in other purposes. The additional baud-rate generator can also be configured to provide a programmable clock output on P1.0. Combined with Timer1 and Timer0, STC12C5A60S2 will be able to provide three individual programmable clock outputs on three general-purpose I/O pins, respectively.

**Mode 0**

Serial data enters and exits through RXD2/P1.2(RXD2/P4.2). TXD2/P1.3(TXD2/P4.3) outputs the shift clock. Eight data bits are transmitted/received with the LSB first. The baud rate is fixed at 1/12 the system clock. Regardless of baud-rate generation, the operation in Mode 0 for S2 UART is the same as the standard UART in Mode 0.

**Mode 1**

10 bits are transmitted through TXD2/P1.3(TXD2/P4.3) or received through RXD2/P1.2(RXD2/P4.2). The frame data includes a start bit(0), 8 data bits and a stop bit(1). One receive, the stop bit goes into S2RB8 in SFR – S2CON. The baud rate is determined by the BRT overflow rate. Regardless of baud-rate generation, the operation in Mode 1 for S2 UART is the same as the standard UART in Mode 1.

\[
\text{Baud rate in mode 1} = \left(2^{S2SMOD}/32\right) \times \text{BRT timer overflow rate}
\]

**Mode 2**

11 bits are transmitted through TXD2/P1.3(TXD2/P4.3) or received through RXD2/P1.2(RXD2/P4.2). The frame data includes a start bit(0), 8 data bits, a programmable 9th bit and a stop bit(1). On transmit, the 9th data bit comes from S2TB8 in S2CON. On receive, the 9th data bit goes into S2RB8 in S2CON. The baud rate is programmable to either 1/32 or 1/64 the system clock cycle. The operation in Mode 2 for S2 UART is the same as the standard UART in Mode 2.

\[
\text{Baud rate in mode 2} = \left(2^{S2SMOD}/64\right) \times \text{SYSclk}
\]

**Mode 3**

Mode 3 is the same as mode 2 except the baud rate is variable.

\[
\text{Baud rate in mode 3} = \left(2^{S2SMOD}/32\right) \times \text{BRT timer overflow rate}
\]

*When S2_P4 bit in AUXR1 register is set, the function of UART2 is redirected to P4.2 for RXD2 and P4.3 for TXD2.*
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Bit Address and Symbol</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRT</td>
<td>Baud-Rate Timer</td>
<td>9CH</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>AUXR</td>
<td>Auxiliary register</td>
<td>8EH</td>
<td><strong>MSB</strong> 80 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>SCON</td>
<td>Serial Control</td>
<td>98H</td>
<td><strong>SM0</strong> 00 <strong>SM1</strong> 00 <strong>SM2</strong> 00 <strong>REN</strong> 00 <strong>TB8</strong> 00 <strong>RB8</strong> 00 <strong>TI</strong> 00 <strong>RI</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>SBUF</td>
<td>Serial Buffer</td>
<td>99H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>PCON</td>
<td>Power Control</td>
<td>87H</td>
<td><strong>SMOD</strong> 00 <strong>SMOD0</strong> 00 <strong>LVDF</strong> 00 <strong>POF</strong> 00 <strong>GF1</strong> 00 <strong>GF0</strong> 00 <strong>PD</strong> 00 <strong>IDL</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IE</td>
<td>Interrupt Enable</td>
<td>A8H</td>
<td><strong>EA</strong> 00 <strong>LVD</strong> 00 <strong>EADC</strong> 00 <strong>ES</strong> 00 <strong>ET1</strong> 00 <strong>EX1</strong> 00 <strong>ET0</strong> 00 <strong>EX0</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IP</td>
<td>Interrupt Priority Low</td>
<td>B8H</td>
<td><strong>PPCA</strong> 00 <strong>PLVD</strong> 00 <strong>PADC</strong> 00 <strong>PS</strong> 00 <strong>PT1</strong> 00 <strong>PX1</strong> 00 <strong>PT0</strong> 00 <strong>PX0</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IPH</td>
<td>Interrupt Priority High</td>
<td>B7H</td>
<td><strong>PPCAH</strong> 00 <strong>PLVDH</strong> 00 <strong>PADC</strong> 00 <strong>PS</strong> 00 <strong>PT1H</strong> 00 <strong>PX1H</strong> 00 <strong>PT0H</strong> 00 <strong>PX0H</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>SADEN</td>
<td>Slave Address Mask</td>
<td>B9H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>SADDR</td>
<td>Slave Address</td>
<td>A9H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>TCON</td>
<td>Timer Control</td>
<td>88H</td>
<td><strong>TF1</strong> 00 <strong>TR1</strong> 00 <strong>TF0</strong> 00 <strong>TR0</strong> 00 <strong>IE1</strong> 00 <strong>IT1</strong> 00 <strong>IE0</strong> 00 <strong>IT0</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>TMOD</td>
<td>Timer Mode</td>
<td>89H</td>
<td><strong>GATE</strong> 00 <strong>C/T</strong> 00 <strong>M1</strong> 00 <strong>M0</strong> 00 <strong>GATE</strong> 00 <strong>C/T</strong> 00 <strong>M1</strong> 00 <strong>M0</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>TL1</td>
<td>Timer Low 1</td>
<td>88H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>TH1</td>
<td>Timer High 1</td>
<td>8DH</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>S2CON</td>
<td>S2 Control</td>
<td>9AH</td>
<td><strong>S2SM0</strong> 00 <strong>S2SM1</strong> 00 <strong>S2SM2</strong> 00 <strong>S2REN</strong> 00 <strong>S2TB8</strong> 00 <strong>S2RB8</strong> 00 <strong>S2TI</strong> 00 <strong>S2RI</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>S2SBUF</td>
<td>S2 Serial Buffer</td>
<td>9BH</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>AUXR1</td>
<td>Auxiliary register1</td>
<td>A2H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IE2</td>
<td>Interrupt Enable 2</td>
<td>AFH</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IP2</td>
<td>2nd Interrupt Priority Low</td>
<td>B5H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>IP2H</td>
<td>2nd Interrupt Priority Low</td>
<td>B6H</td>
<td><strong>MSB</strong> 90 <strong>Lsb</strong> 00</td>
<td>0000 0000B</td>
</tr>
<tr>
<td>WAKE_CLKO</td>
<td>CLK_Output Power down</td>
<td>8FH</td>
<td><strong>PCAWAKE</strong> 00 <strong>RAR_PIN_IE</strong> 00 <strong>T1_PIN_IE</strong> 00 <strong>T0_PIN_IE</strong> 00 <strong>LVD_WAKE</strong> 00 <strong>BRTCLK0</strong> 00 <strong>TICLK0</strong> 00 <strong>T5CLK0</strong> 00</td>
<td>0000 0000B</td>
</tr>
</tbody>
</table>
There are several special function registers which should be understood by users before using the secondary UART.

**S2CON register**

<table>
<thead>
<tr>
<th>bit</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>S2SM0</td>
<td>S2SM1</td>
<td>S2SM2</td>
<td>S2REN</td>
<td>S2TB8</td>
<td>S2RB8</td>
<td>S2TI</td>
<td>S2RI</td>
</tr>
<tr>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

S2SM0, S2SM1: Serial Port Mode Bit 0/1.

S2SM0, S2SM1

- **Description**: Baud rate
- **Value**:
  - 0 0: 8-bit shift register, SYSclock/12
  - 0 1: 8-bit UART, variable
  - 1 0: 9-bit UART, SYSclock/64 or SYSclock/32
  - 1 1: 9-bit UART, variable

S2SM2: Enable the automatic address recognition feature in mode 2 and 3. If S2SM2=1, S2 RI will not be set unless the received 9th data bit is 1, indicating an address, and the received byte is a Given or Broadcast address. In mode 1, if S2SM2=1 then RI will not be set unless a valid stop bit was received, and the received byte is a Given or Broadcast address.

S2REN: Enable the serial port reception. When set, enable serial reception. When clear, disable the secondary serial port reception.

S2TB8: The 9th data bit which will be transmitted in mode 2 and 3.

S2RB8: In mode 2 and 3, the received 9th data bit will go into this bit.

S2TI: Transmit interrupt flag. After a transmitting has been finished, the hardware will set this bit.

S2RI: Receive interrupt flag. After reception has been finished, the hardware will set this bit.

**S2BUF register**

It is used as the buffer register in transmission and reception.

**BRT register**

It is used as the reload register for generating the baud-rate of the secondary UART.

**Auxiliary Interrupt Enable register (IE2)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>ESPI</td>
<td>ES2</td>
</tr>
<tr>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

B7-B2: Reserved

ESPI: When set, enables SPI interrupt.

ES2: When set, enables UART2 interrupt.

**Interrupt Priority Low register 2(IP2)**

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>PSPI</td>
<td>PS2</td>
</tr>
<tr>
<td>LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

B7-B2: Reserved

PSPI: SPI interrupt priority bit.

PS2: UART2 interrupt priority bit.
### AUXR register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
<td>S2SMOD</td>
<td>BRTx12</td>
<td>EXTRAM</td>
<td>S1BRS</td>
</tr>
</tbody>
</table>

- **T1x12**
  - 0: The clock source of Timer 1 is SYSclk/12.
  - 1: The clock source of Timer 1 is SYSclk.

- **UART_M0x6**
  - 0: Clear to select SYSclk/12 as the baud rate for UART Mode 0.
  - 1: Set to select SYSclk/2 as the baud rate for UART Mode 0.

- **BRTR**: Independent Baud-rate generator control bit.
  - 0: The independent baud-rate generator is stopped
  - 1: The independent baud-rate generator is stopped

- **S2SMOD**
  - 0: Default.
  - 1: The baud-rate UART2(S2) is doubled.

- **BRTx12**
  - 0: The independent baud-rate is incremented every 12 system clocks.
  - 1: The independent baud-rate is incremented every system clock.

- **S1BRS**
  - 0: select Timer 1 as the baud-rate generator of the enhanced UART.
  - 1: Timer 1 is replaced by the independent baud-rate generator for use of the enhanced UART. In other word, T1 is released to use in other functions.

### AUXR1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
</tr>
</tbody>
</table>

- **PCA_P4**
  - 0: Default.
  - 1: The PCA function in P1 [4:2] is switched to P4[3:1].

- **SPI_P4**
  - 0: Default.
  - 1: The SPI function in P1[7:4] is redirected to P4[3:0].

- **S2_P4**
  - 0: Default.
  - 1: The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].

- **GF2**: General Flag. It can be used by software.

- **ADRJ**
  - 0: The 10-bit conversion result of ADC is arranged as {ADC[7:0], ADCVL[1:0]}.
  - 1: The 10-bit conversion result is right-justified, {ADCV[1:0], ADCVL[7:0]}.

- **DPS**
  - 0: Default.
  - 1: The secondary DPTR is switched to use.
There is an example program for the secondary UART communication which is written in C language and shown as below.

```c
#include<reg52.h>
#include<intrins.h>
sfr S2CON = 0x9A;
//S2SM0, S2SM1, S2SM2, S2REN, S2TB8, S2RB8, S2TI, S2RI
sfr IE2 = 0xAF;
//X, X, X, X, X, X, ESPI, ES2
sfr S2BUF = 0x9B;
sfr AUXR = 0x8E;
sfr BRT = 0x9C;
sfr IAP_CONTR = 0xC7;
sfr CCON = 0xD8;
sfr CMOD = 0xD9;
sfr CL = 0xE9;
sfr CH = 0xF9;
sfr CCAP0L = 0xEA;
sfr CCAP0H = 0xFA;
sfr CCAPM0 = 0xDA;
sfr CCAPM1 = 0xDB;
sfr CR = 0xDE;
sbit MCU_Start_LED = P1^7;
sbit S2_Interrupt_Receive_LED = P1^4;
//unsigned char self_command_array[4] = {0x22, 0x33, 0x44, 0x55};
#define RELOAD_COUNT   0xfb  //18.432MHz, 12T, SMOD=0, 9600bps
//# define RELOAD_COUNT  0xf6  //18.432MHz, 12T, SMOD=0, 4800bps
//# define RELOAD_COUNT  0xec  //18.432MHz, 12T, SMOD=0, 2400bps
//# define RELOAD_COUNT  0xd8  //18.432MHz, 12T, SMOD=0, 1200bps
void serial_port_one_initial();
void send_UART_one(unsigned char);
void UART_one_Interrupt_Receive(void);

void serial_port_two_initial();
void send_UART_two(unsigned char);
void UART_two_Interrupt_Receive(void);

void soft_reset_to_ISP_Monitor(void);
void delay(void);
void display_MCU_Start_LED(void);
void send_PWM(void);

void main(void)
{
    unsigned int array_point = 0;
    unsigned char xdata Test_array_ont[512] =
    {
    
```
0x00, 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07,
0x08, 0x09, 0x0a, 0x0b, 0x0c, 0x0d, 0x0e, 0x0f,
0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17,
0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e, 0x1f,
0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27,
0x28, 0x29, 0x2a, 0x2b, 0x2c, 0x2d, 0x2e, 0x2f,
0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37,
0x38, 0x39, 0x3a, 0x3b, 0x3c, 0x3d, 0x3e, 0x3f,
0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47,
0x48, 0x49, 0x4a, 0x4b, 0x4c, 0x4d, 0x4e, 0x4f,
0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57,
0x58, 0x59, 0x5a, 0x5b, 0x5c, 0x5d, 0x5e, 0x5f,
0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67,
0x68, 0x69, 0x6a, 0x6b, 0x6c, 0x6d, 0x6e, 0x6f,
0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77,
0x78, 0x79, 0x7a, 0x7b, 0x7c, 0x7d, 0x7e, 0x7f,
0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87,
0x88, 0x89, 0x8a, 0x8b, 0x8c, 0x8d, 0x8e, 0x8f,
0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97,
0x98, 0x99, 0x9a, 0x9b, 0x9c, 0x9d, 0x9e, 0x9f,
0xa0, 0xa1, 0xa2, 0xa3, 0xa4, 0xa5, 0xa6, 0xa7,
0xa8, 0xa9, 0xaa, 0xab, 0xac, 0xad, 0xae, 0xaf,
0xb0, 0xb1, 0xb2, 0xb3, 0xb4, 0xb5, 0xb6, 0xb7,
0xb8, 0xb9, 0xba, 0xbb, 0xbc, 0xbd, 0xbe, 0xbf,
0xc0, 0xc1, 0xc2, 0xc3, 0xc4, 0xc5, 0xc6, 0xc7,
0xc8, 0xc9, 0xca, 0xcb, 0xcc, 0xcd, 0xce, 0xcf,
0xd0, 0xd1, 0xd2, 0xd3, 0xd4, 0xd5, 0xd6, 0xd7,
0xd8, 0xd9, 0xda, 0xdb, 0xdc, 0xdd, 0xde, 0xdf,
0xe0, 0xe1, 0xe2, 0xe3, 0xe4, 0xe5, 0xe6, 0xe7,
0xe8, 0xe9, 0xea, 0xeb, 0xec, 0xed, 0xee, 0xef,
0xf0, 0xf1, 0xf2, 0xf3, 0xf4, 0xf5, 0xf6, 0xf7,
0xf8, 0xf9, 0xfa, 0xfb, 0xfc, 0xfd, 0xfe, 0xff,
};
unsigned char  i = 0;
serial_port_one_initial( );   //Initialize the major UART
serial_port_two_initial( );   //Initialize the secondary UART(S2)
display_MCU_Start_LED( );   //Open MCU-Start-LED, MCU start to work

send_UART_two(0x55);   //send data—0x55 by the secondary UART
send_UART_two(0xaa);   //send data—0xaa by the secondary UART

for (array_point = 0; array_point<512; array_point++)
{
    send_UART_two (Test array_one[array_point]);
}

send_UART_one(0x34);   //send data—0x34 by the major UART
send_UART_one(0xa7);   //send data—0xa7 by the major UART

for (array_point = 0; array_point<512; array_point++)
{
    send_UART_one (Test array_one[array_point]);
}

send_PWM( );   //6kHz PWM, 50% duty
while(1)
}

void serial_port_one_initial( )
{
    SCON  = 0x50;   //0101,0000  8-bit variable baud rate, no parity bit
    // TMOD = 0x21;   //0011, 0001  set Timer 1 for 8-bit auto-reload mode
    // TH1  = RELOAD_COUNT;   //Load Timer 1 auto-reload value
    // TL1  = RELOAD_COUNT;

}
// TR1 = 1; // Enable Timer 1
BRT = RELOAD_COUNT;
// BRTR = 1, S1BRS = 1, EXTRAM = 1, ENABLE EXTRAM
AUXR = 0x11; // T0x12, T1x12, UART_M0x6, BRTR, S2SMOD, BRTx12, EXTRAM, S1BRS
ES = 1; // Enable serial port interrupt
EA = 1; // Set the global enable bit

} void serial_port_two_initial()
{
    //sfr SCON = 0x98;
    //SM0, SM1, SM2, REN, TB8, RB8, TI, RI

    //sfr S2CON = 0x9A;
    //S2SM0, S2SM1, S2SM2, S2REN, S2TB8, S2RB8, S2TI, S2RI
    //sfr S2BUF = 0x9B;
    //sfr IE2 = 0xAF;
    //X, X, X, X, X, X, ESPI, ES2
    S2CON = 0x50; // 0101, 0000 8-bit variable baud rate, no parity bit,
    BRT = RELOAD_COUNT;
    // BRTR = 1, S1BRS = 1, EXTRAM = 0, ENABLE EXTRAM
    AUXR = 0x11; // T0x12, T1x12, UART_M0x6, BRTR, S2SMOD, BRTx12, EXTRAM, S1BRS
    ES = 1; // Enable the major UART interrupt
    // ES2 = 1;
    IE2 = 0x01; // Enable the secondary UART interrupt, ES2 = 1
    EA = 1; // Set the global enable bit

} void send_UART_one(unsigned char i)
{
    ES = 0; //Disable serial port interrupt
    TI = 0; //Clear serial port transmit interrupt flag
    SUBF = i;
    while (TI == 0); //Wait to finish transmitting
    TI = 0; //Clear serial port transmit interrupt flag
    ES = 1; //Enable serial port interrupt

} void send_UART_two(unsigned char i)
{
    //sfr SCON = 0x98;
    //SM0, SM1, SM2, REN, TB8, RB8, TI, RI

    //sfr S2CON = 0x9A;
    //S2SM0, S2SM1, S2SM2, S2REN, S2TB8, S2RB8, S2TI, S2RI
    //sfr S2BUF = 0x9B;
    //sfr IE2 = 0xAF;
    //X, X, X, X, X, X, ESPI, ES2
unsigned char temp = 0;
// Disable the major UART interrupt
ES = 0;
// Disable the secondary UART interrupt, ES2=0
IE2 = 0x00;
// Clear the major UART transmit interrupt flag
S2CON = S2CON & 0xFD;  //B' 11111101,Clear the secondary UART transmit interrupt flag
// TI = 0;   //Clear the major UART transmit interrupt flag
S2BUF = i;
S2CON = S2CON & 0xFD;  //B' 11111101,Clear the secondary UART transmit interrupt flag
// TI = 0;   //Clear the major UART transmit interrupt flag
while(TI == 0);
do
{
    temp = S2CON;
    temp = temp & 0x02;
}while(temp == 0);
// Enable the major UART interrupt
// ES2 = 1;
IE2 = 0x01;   // Enable the secondary UART interrupt, ES2=1
void UART_one_Interrupt_Receive(void) interrupt 4
{
    unsigned char k = 0;
    if(RI ==1)
    {
        RI = 0;
        k = SBUF;
        if(k==Self_Define_ISP_Download_Command)  //Self-define download-command
        {
            delay();  // to delay 1s is enough
            delay();  // to delay 1s is enough
            soft_reset_to_ISP_Monitor( );  //soft-reset to ISP-monitor
        }
        send_UART_one(k+1);
    }
    else
    {
        TI =0;
    }
}
void UART_two_Interrupt_Receive(void) interrupt 8
{
    //sfr SCON = 0x98;
    //SM0, SM1, SM2, REN, TB8, RB8, TI, RI
    //sfr S2CON = 0x9A;
    //S2SM0, S2SM1, S2SM2, S2REN, S2TB8, S2RB8, S2TI, S2RI
    //sfr S2BUF = 0x9B;
    //sfr IE2 = 0xAF;
    //X, X, X, X, X, ESP1, ES2
unsigned char k = 0;
k = S2CON;
k = k & 0x01;
//if (S2RI == 1)
if (k==1)
{
    //RI = 0;
    S2CON = S2CON & 0xFE;  //1111,1110
    S2_Interrupt_Receive_LED = 0;
    k = S2BUF;
    if (k==Self_Define_ISP_Download_Command)     //Self-define ISP download-command
    {
        delay( );  //to delay 1s is enough
        delay( );  //to delay 1s is enough
        soft_reset_to_ISP_Monitor( );  //soft-reset to ISP-monitor
    }
    send_UART_two(k+1);
}
else
{
    //TI = 0;
    S2CON = S2CON & 0xFD;    //1111, 1101
}
}

void soft_reset_to_ISP_Monitor (void)
{
    IAP_CONTR = 0x60;  //0110,0000    soft-reset to ISP-monitor
}

void delay (void)
{
    unsigned int j = 0;
    unsigned int g = 0;
    for(j=0; j<5; j++)
    {
        for(g=0; g<60000; g++)
        {
            _nop_( );
            _nop_( );
            _nop_( );
            _nop_( );
            _nop_( );
        }
    }
}
void display_MCU_Start_LED(void)
{
    //sbit MCU_Start_LED = P1^7;
    for (i=0; i<1; i++)
    {
        MCU_Start_LED = 0; //turn on MCU-Start-LED
        delay();
        MCU_Start_LED = 1; //turn off MCU-Start-LED
        delay();
        MCU_Start_LED = 0; //turn on MCU-Start-LED
    }
}

void send_PWM (void)
{
    CMOD = 0x00;       //CIDL--------------CPS1 CPS2 ECF   Setup PCA Timer
    //CPS1 CPS2 = 00, SYScK/12 is PCA/PWM clock
    //18432000/12/256 = 6000
    CL = 0x00;
    CH = 0x00;
    CCAP0L = 0x80; //Set the initial value same as CCAP0H
    CCAP0H = 0x80; //50% Duty Cycle
    CCAPM0= 0x42; //0100,0010 Setup PCA module 0 in 8-bit PWM, P3.7
    CR = 1 //Setup PCA/PWM Timer
}

The following program is another program for the secondary UART communication, but written in assembly language rather than in C language.
S2CON    EQU  9AH
;S2SM0, S2SM1, S2SM2, S2REN, S2TB8, S2RB8, S2TI, S2RI
IE2      EQU  0AFH
;X, X, X, X, X, X, ESPI, ES2
S2BUF    EQU  9BH

AUXR     EQU  8EH
BRT      EQU  9CH
IAP_CONTR EQU  0C7H

RELAOD_COUNT EQU  0FBH       ;18.432MHz, 12T, SMOD = 0, 9600bps
;RELAOD_COUNT EQU  0F6H       ;18.432MHz, 12T, SMOD = 0, 4800bps
;RELAOD_COUNT EQU  0ECH       ;18.432MHz, 12T, SMOD = 0, 2400bps
;RELAOD_COUNT EQU  0D8H       ;18.432MHz, 12T, SMOD = 0, 1200bps

;---------------------------------------------------------------------------------------------------------------------
ORG 0000H
LJMP MAIN

ORG 0043H
LJMP UART_two_Interrupt_Receive

ORG 0100H
MAIN:
MOV SP, #0C0H
LCALL UART2_Initial

MOV 11H, #55H
LCALL send_UART_two

MOV 11H, #0AAH
LCALL send_UART_two

SJMP $

UART2_Initial:
PUSH ACC
MOV SCON, #50H ;0101,0000 8-bit variable baud rate, no parity
MOV BRT, #RELOAD_COUNT;
MOV AUXR, #11H
;T0x12,T1x12,UART_M0x6,BRTR,S2SMOD,BRTx12,EXTRAM,S1BRS
;BRTR=1, S1BRS=1, EXTRAM=0 ENABLE EXTRAM
MOV IE2, #01H ;Enable the secondary UART interrupt, ES2=1
SETTB EA ;Set the global enable bit
POP ACC
RET

;---------------------------------------------------------------------------------------------------------------------------------------
send_UART_two:
PUSH ACC
MOV IE2, #00H ;Disable the secondary UART interrupt, ES2=0
MOV A, S2CON ;1111,1101, Clear secondary UART transimit interrupt flag
ANL A, #0FDH
MOV S2CON, A
MOV S2BUF, 11H

UART2_Send_Wait:
MOV A, S2CON
ANL A, #02H ;0000,0010
CJNE A, #02H, UART_Send_Wait
MOV A, S2CON
ANL A, #0FDH ;1111,1101, Clear secondary UART transimit interrupt flag
MOV S2CON, A
MOV IE2, #01H ;Enable the secondary UART interrupt, ES2=1
POP ACC
RET

;---------------------------------------------------------------------------------------------------------------------------------------
UART_two_Interrupt_Receive:

PUSS     ACC
MOV    A,        S2CON
ANL    A,       #01H
CJNE   A,   #01H,  CLEAR_S2TI_RETI

MOV    A,        S2CON
ANL    A,      #0FEH    ;1111,1110
MOV    S2CON,  A

MOV 11H,        S2BUF
INC    11H
LCALL  send_UART_two
POP    ACC
RETI

CLEAR_S2TI_RETI:

MOV    A,        S2CON
ANL    A,       #0FDH    ;1111,1101
MOV    S2CON,  A

POP    ACC
RETI

END
Chapter 9. Analog to Digital Converter

9.1 ADC Structure

The ADC on STC12C5A60S2 is an 10-bit resolution, successive-approximation approach, medium-speed A/D converter. $V_{REFP}$/$V_{REFM}$ is the positive/negative reference voltage input for internal voltage-scaling DAC use, the typical sink current on it is 600μA ~ 1mA. For STC12C5A60S2, these two references are internally tied to VCC and GND separately.

Conversion is invoked since ADC_STRAT(ADC_CONTR.3) bit is set. Before invoking conversion, ADC_POWER/ADC_CONTR.7 bit should be set first in order to turn on the power of analog front-end in ADC circuitry. Prior to ADC conversion, the desired I/O ports for analog inputs should be configured as input-only or open-drain mode first. The converter takes around a fourth cycles to sample analog input data and other three fourths cycles in successive-approximation steps. Total conversion time is controlled by two register bits – SPEED1 and SPEED0. Eight analog channels are available on P1 and only one of them is connected to the comparator depending on the selection bits {CHS2,CHS1,CHS0}. When conversion is completed, the result will be saved onto {ADC_RES,ADC_RESL[1:0]} register if AUXR1.2(ADRJ )=0 or saved onto {ADC_RES[1:0],ADC_RESL} if ADRJ=1 . After the result are completed and saved, ADC_FLAG is also set. ADC_FLAG associated with its enable register IE.5(EADC). ADC_FLAG should be cleared in software. The ADC interrupt service routine vectors to 2Bh . When the chip enters idle mode or power-down mode, the power of ADC is gated off by hardware.

Conversion result = $1024 \times \frac{ Vin - V_{REFM} }{ V_{REFP} - V_{REFM} }$
9.2 Register for ADC

<table>
<thead>
<tr>
<th>SFR Name</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1ASF</td>
<td>P17ASF</td>
<td>P16ASF</td>
<td>P15ASF</td>
<td>P14ASF</td>
<td>P13ASF</td>
<td>P12ASF</td>
<td>P11ASF</td>
<td>P10ASF</td>
</tr>
</tbody>
</table>

P1xASF
0 : = Keep P1.x as general-purpose I/O function.
1 : = Set P1.x as ADC input channel-x

ADC_CONTR( ADC Control register )

<table>
<thead>
<tr>
<th>bit name</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC_POWER</td>
<td>SPEED1</td>
<td>SPEED0</td>
<td>ADC_FLAG</td>
<td>ADC_START</td>
<td>CHS2</td>
<td>CHS1</td>
<td>CHS0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ADC_POWER : When clear shut down the power of ADC block. When set turn on the power of ADC block.
SPEED1, SPEED0 : Conversion speed selection.
00 : 540 clock cycles are needed for a conversion.
01 : 360 clock cycles are needed for a conversion.
10 : 180 clock cycles are needed for a conversion.
11 : 90 clock cycles are needed for a conversion.

ADC_FLAG : ADC interrupt flag. It will be set by the device after the device has finished a conversion, and should be cleared by the user's software.

ADC_START : ADC start bit, which enable ADC conversion. It will automatically cleared by the device after the device has finished the conversion.

CHS2 ~ CHS0 : Used to select one analog input source from 8 channels.

<table>
<thead>
<tr>
<th>CHS2</th>
<th>CHS1</th>
<th>CHS0</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>P1.0 (default) as the A/D channel input</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>P1.1 as the A/D channel input</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>P1.2 as the A/D channel input</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>P1.3 as the A/D channel input</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>P1.4 as the A/D channel input</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>P1.5 as the A/D channel input</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>P1.6 as the A/D channel input</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>P1.7 as the A/D channel input</td>
</tr>
</tbody>
</table>

Note : The corresponding bits in P1ASF should be configured correctly before starting A/D conversion. The specified P1ASF bits should be set corresponding with the desired channels.
ADC_RES (ADC result register)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The ADC_RES is the final result from the A/D conversion.

ADC_RESL (Low Byte of ADC result register)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AUXR1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
<td></td>
</tr>
</tbody>
</table>

PCA_P4
0 : Default.
1 : The PCA function in P1[4:2] is switched to P4[3:1].

SPI_P4
0 : Default.
1 : The SPI function in P1[7:4] is redirected to P4[3:0].

S2_P4
0 : Default.
1 : The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].

GF2 : General Flag. It can be used by software.

ADRJ
0 : The 10-bit conversion result of ADC is arranged as {ADC_RES[7:0], ADC_RESL[1:0]}.
1 : The 10-bit conversion result is right-justified, {ADC_RES[1:0], ADC_RESL[7:0]}.

DPS
0 : Default.
1 : The secondary DPTR is switched to use.
### IE: Interrupt Enable Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EA</td>
<td>IE.7</td>
<td>EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.</td>
</tr>
<tr>
<td>ELVD</td>
<td>IE.6</td>
<td>Low voltage detection interrupt enable bit.</td>
</tr>
<tr>
<td>EADC</td>
<td>IE.5</td>
<td>ADC interrupt enable bit.</td>
</tr>
<tr>
<td>ES</td>
<td>IE.4</td>
<td>Serial Port interrupt enable bit.</td>
</tr>
<tr>
<td>ET1</td>
<td>IE.3</td>
<td>Timer 1 interrupt enable bit.</td>
</tr>
<tr>
<td>EX1</td>
<td>IE.2</td>
<td>External interrupt 1 enable bit.</td>
</tr>
<tr>
<td>ET0</td>
<td>IE.1</td>
<td>Timer 0 interrupt enable bit.</td>
</tr>
<tr>
<td>EX0</td>
<td>IE.0</td>
<td>External interrupt 0 enable bit.</td>
</tr>
</tbody>
</table>

### IP: Interrupt Priority Register

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Position</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PPCA</td>
<td>IP.7</td>
<td>PCA interrupt priority bit.</td>
</tr>
<tr>
<td>PLVD</td>
<td>IP.6</td>
<td>Low voltage detection interrupt priority bit.</td>
</tr>
<tr>
<td>PADC</td>
<td>IP.5</td>
<td>ADC interrupt priority bit.</td>
</tr>
<tr>
<td>PS</td>
<td>IP.4</td>
<td>Serial Port interrupt priority bit.</td>
</tr>
<tr>
<td>PT1</td>
<td>IP.3</td>
<td>Timer 1 interrupt priority bit.</td>
</tr>
<tr>
<td>PX1</td>
<td>IP.2</td>
<td>External interrupt 1 priority bit.</td>
</tr>
<tr>
<td>PT0</td>
<td>IP.1</td>
<td>Timer 0 interrupt priority bit.</td>
</tr>
<tr>
<td>PX0</td>
<td>IP.0</td>
<td>External interrupt 0 priority bit.</td>
</tr>
</tbody>
</table>
9.3 A/D application circuit for key scan

9.4 A/D reference voltage source

STC12C5Axx series ADC reference voltage is from MCU power supply voltage directly, so it can work without an external reference voltage source. If the required precision is relatively high, then you maybe using a stable reference voltage source, in order to calculate the operating voltage VCC, then calculate the ADC exact value. For example, you can connect a 1.25V(or 1.00V, ect…) to ADC channel 7, according to the conversion result, you can get the actual VCC voltage, thus you can calculate other 7 channels ADC results.
9.5 Program using interrupts to demonstrate A/D Conversion

There are two example procedures using interrupts to demonstrate A/D conversion, one written in assembly language and the other in C language.

Assembly language code listing:

```assembly
;--------------------------------------------------------------------
;* --- STC MCU International Limited ---------------------------------
;* --- STC 1T Series MCU A/D Conversion Demo ------------------------
;* --- Mobile: (86)13922805190 ----------------------------------------
;* --- Fax: 86-755-82944243 ------------------------------------------
;* --- Tel: 86-755-82948412 -------------------------------------------
;* --- Web: www.STCMCU.com -------------------------------------------
;* If you want to use the program or the program referenced in the   *
;* article, please specify in which data and procedures from STC      *
;*---------------------------------------------------------------------

Declare SFR associated with the ADC

ADC_CONTR    EQU  0BCH  ;ADC control register
ADC_RES      EQU  0BDH  ;ADC high 8-bit result register
ADC_LOW2     EQU  0BEH  ;ADC low 2-bit result register
P1ASF        EQU  09DH   ;P1 secondary function control register

;Define ADC operation const for ADC_CONTR
ADC_POWER    EQU  80H  ;ADC power control bit
ADC_FLAG     EQU  10H  ;ADC complete flag
ADC_START    EQU  08H  ;ADC start control bit
ADC_SPEEDLL  EQU  00H  ;540 clocks
ADC_SPEEDL   EQU  20H  ;360 clocks
ADC_SPEEDH   EQU  40H  ;180 clocks
ADC_SPEEDHH  EQU  60H  ;90 clocks
ADCCH        DATA  20H  ;ADC channel NO.

ORG    0000H
LJMP   MAIN

ORG    002BH
LJMP   ADC_ISR

ORG    0100H
MAIN:
MOV    SP, #3FH
MOV    ADCCH, #0
LCALL  INIT_UART ;Init UART, use to show ADC result
LCALL  INIT_ADC ;Init ADC sfr
MOV    IE, #0A0H ;Enable ADC interrupt
;and Open master interrupt switch
SJMP   $
```
; ADC interrupt service routine
; -----------------------------------------

ADC_ISR:
    PUSH ACC
    PUSH PSW
    ANL ADC_CONTR, #NOT ADC_FLAG ;Clear ADC interrupt flag
    MOV A, ADCCH
    LCALL SEND_DATA ;Send channel NO.
    MOV A, ADC_RES ;Get ADC high 8-bit result
    LCALL SEND_DATA ;Send to UART

; if you want show 10-bit result, uncomment next 2 lines
;
    MOV A, ADC_LOW2 ;Get ADC low 2-bit result
    LCALL SEND_DATA ;Send to UART

    INC ADCCH
    MOV A, ADCCH
    ANL A, #07H
    MOV ADCCH, A
    ORL A, #ADC_POWER | ADC_SPEEDLL | ADC_START
    MOV ADC_CONTR, A ;ADC power-on delay
    and re-start A/D conversion

    POP PSW
    POP ACC
    RETI

; ---------------------------------------

INIT_ADC:
    MOV P1ASF, #0FFH ;Set all P1 as analog input port
    MOV ADC_RES, #0 ;Clear previous result
    MOV A, ADCCH
    ORL A, #ADC_POWER | ADC_SPEEDLL | ADC_START
    MOV ADC_CONTR, A ;ADC power-on delay
    and Start A/D conversion

    MOV A, #2
    LCALL DELAY
    RET

; ---------------------------------------

INIT_UART:
    MOV SCON, #5AH ;8 bit data ,no parity bit
    MOV TMOD, #20H ;T1 as 8-bit auto reload
    MOV A, #5 ;Set Uart baudrate -(18432000/12/32/9600)
    MOV TH1, A ;Set T1 reload value
    MOV TL1, A
    SETB TR1 ;T1 start running
    RET
C language code listing:

```c
#include "reg51.h"
#include "intrins.h"

#define FOSC 18432000L
#define BAUD 9600

typedef unsigned char BYTE;
typedef unsigned int WORD;
```
/*Declare SFR associated with the ADC*/
sfr  ADC_CONTR = 0xBC;              //ADC control register
sfr  ADC_RES = 0xBD;                //ADC hight 8-bit result register
sfr  ADC_LOW2 = 0xBE;               //ADC low 2-bit result register
sfr  P1ASF = 0x9D;                  //P1 secondary function control register

/*Define ADC operation const for ADC_CONTR*/
#define ADC_POWER 0x80            //ADC power control bit
#define ADC_FLAG 0x10             //ADC complete flag
#define ADC_START 0x08             //ADC start control bit
#define ADC_SPEEDLL 0x00             //540 clocks
#define ADC_SPEEDL 0x20             //360 clocks
#define ADC_SPEEDH 0x40             //180 clocks
#define ADC_SPEEDHH 0x60             //90 clocks

void InitUart();
void SendData(BYTE dat);
void Delay(WORD n);
void InitADC();
BYTE ch = 0;                          //ADC channel NO.

void main()
{
    InitUart();                       //Init UART, use to show ADC result
    InitADC();                        //Init ADC sfr
    IE = 0xa0;                        //Enable ADC interrupt and Open master interrupt switch
                                        //Start A/D conversion
    while (1);
}

/*-----------------------------------------
ADC interrupt service routine
--------------------------------------------*/
void adc_isr( ) interrupt 5 using 1
{
    ADC_CONTR &= !ADC_FLAG;          //Clear ADC interrupt flag
    SendData(ch);                     //Show Channel NO.
    SendData(ADC_RES);               //Get ADC high 8-bit result and Send to UART
    //if you want show 10-bit result, uncomment next line
    //SendData(ADC_LOW2);              //Show ADC low 2-bit result

    if (++ch > 7) ch = 0;             //switch to next channel
    ADC_CONTR = ADC_POWER | ADC_SPEEDLL | ADC_START | ch;
}
/*-----------------------------------
Initial ADC sfr
-------------------------------------*/
void InitADC()
{
    P1ASF = 0xff;                      //Set all P1 as analog input port
    ADC_RES = 0;                      //Clear previous result
    ADC_CONTR = ADC_POWER | ADC_SPEEDLL | ADC_START | ch;
    Delay(2);                          //ADC power-on delay and Start A/D conversion
}

;/*-----------------------------------
Initial UART
--------------------------------------*/
void InitUart()
{
    SCON = 0x5a;                       //8 bit data ,no parity bit
    TMOD = 0x20;                       //T1 as 8-bit auto reload
    TH1 = TL1 = -(FOSC/12/32/BAUD);   //Set Uart baudrate
    TR1 = 1;                           //T1 start running
}

;/*-------------------------------------
Send one byte data to PC
Input: dat (UART data)
Output:-
-----------------------------------------*/
void SendData(BYTE dat)
{
    while (!TI);                       //Wait for the previous data is sent
    TI = 0;                            //Clear TI flag
    SBUF = dat;                        //Send current data
}

;/*----------------------------------------
Software delay function
-------------------------------------------*/
void Delay(WORD n)
{
    WORD x;

    while (n--)
    {
        x = 5000;
        while (x--);
    }
}
9.6 Program using polling to demostrate A/D Conversion

There are two example procedures using inquiry to demostrate A/D conversion, one written in assembly language and the other in C language.

Assembly language code listing:

```assembly
; Declare SFR associated with the ADC
ADC_CONTR EQU 0BCH ; ADC control register
ADC_RES EQU 0BDH ; ADC high 8-bit result register
ADC_LOW2 EQU 0BEH ; ADC low 2-bit result register
P1ASF EQU 09DH ; P1 secondary function control register

/* Define ADC operation const for ADC_CONTR */
ADC_POWER EQU 80H ; ADC power control bit
ADC_FLAG EQU 10H ; ADC complete flag
ADC_START EQU 08H ; ADC start control bit
ADC_SPEEDLL EQU 00H ; 540 clocks
ADC_SPEEDL EQU 20H ; 360 clocks
ADC_SPEEDH EQU 40H ; 180 clocks
ADC_SPEEDHH EQU 60H ; 90 clocks
```

```assembly
ORG 0000H
LJMP MAIN
```

```assembly
ORG 0100H
MAIN:
LCALL INIT_UART ; Init UART, use to show ADC result
LCALL INIT_ADC ; Init ADC sfr
```

```assembly
NEXT:
MOV A, #0
LCALL SHOW_RESULT ; Show channel0 result
MOV A, #1
LCALL SHOW_RESULT ; Show channel1 result
MOV A, #2
LCALL SHOW_RESULT ; Show channel2 result
MOV A, #3
LCALL SHOW_RESULT ; Show channel3 result
```
MOV A, #4
LCALL SHOW_RESULT ;Show channel4 result
MOV A, #5
LCALL SHOW_RESULT ;Show channel5 result
MOV A, #6
LCALL SHOW_RESULT ;Show channel6 result
MOV A, #7
LCALL SHOW_RESULT ;Show channel7 result
SJMP NEXT

;Send ADC result to UART
;Input: ACC (ADC channel NO.)
;Output: -

SHOW_RESULT:
  LCALL SEND_DATA ;Show Channel NO.
  LCALL GET_ADC_RESULT ;Get high 8-bit ADC result
  LCALL SEND_DATA ;Show result
  //if you want show 10-bit result, uncomment next 2 lines
  ;
  ;  MOV A, ADC_LOW2 ;Get low 2-bit ADC result
  ;
  ;  LCALL SEND_DATA ;Show result
 RET

;Read ADC conversion result
;Input: ACC (ADC channel NO.)
;Output: ACC (ADC result)

GET_ADC_RESULT:
  ORL A, #ADC_POWER | ADC_SPEEDLL | ADC_START
  MOV ADC_CONTR,A ;Start A/D conversion
  NOP ;Must wait before inquiry
  NOP
  NOP
  NOP
  WAIT:
    MOV A,ADC_CONTR ;Wait complete flag
    JNB ACC.4, WAIT ;ADC_FLAG(ADC_CONTR.4)
    ANL ADC_CONTR, #NOT ADC_FLAG ;Clear ADC_FLAG
    MOV A, ADC_RES ;Return ADC result
    RET

;Initial ADC sfr

INIT_ADC:
  MOV P1ASF, #OFFH ;Open 8 channels ADC function
  MOV ADC_RES, #0 ;Clear previous result
  MOV ADC_CONTR, #ADC_POWER | ADC_SPEEDLL
  MOV A, #2 ;ADC power-on and delay
  LCALL DELAY
  RET
INIT_UART:
    MOV    SCON, #5AH           ;8 bit data, no parity bit
    MOV    TMOD, #20H          ;T1 as 8-bit auto reload
    MOV    A, #-5              ;Set Uart baudrate -(18432000/12/32/9600)
    MOV    TH1, A               ;Set T1 reload value
    MOV    TL1, A
    SETB   TR1                     ;T1 start running
    RET

SEND_DATA:
    NB    TI, $                  ;Wait for the previous data is sent
    CLR    TI                      ;Clear TI flag
    MOV    SBUF, A                 ;Send current data
    RET

DELAY:
    MOV    R2, A
    CLR    A
    MOV    R0, A
    MOV    R1, A
    DJNZ   R0, DELAY1
    DJNZ   R1, DELAY1
    DJNZ   R2, DELAY1
    RET
    END

C language code listing:
/*-----------------------------*/
/* --- STC MCU International Limited -------------------------------*/
/* --- STC 1T Series MCU A/D Conversion Demo -----------------------*/
/* --- Mobile: (86)13922805190 -----------------------------------------------*/
/* --- Fax: 86-755-82944243 -----------------------------------------------*/
/* --- Tel: 86-755-82948412 -----------------------------------------------*/
/* --- Web: www.STCMCU.com -----------------------------------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*-------------------------------------------------------------------*/
#include "reg51.h"
#include "intrins.h"

#define FOSC 18432000L
#define BAUD 9600

typedef unsigned char BYTE;
typedef unsigned int WORD;

/*Declare SFR associated with the ADC */
sfr ADC_CONTR = 0xBC; //ADC control register
sfr ADC_RES = 0xBD; //ADC high 8-bit result register
sfr ADC_LOW2 = 0xBE; //ADC low 2-bit result register
sfr P1ASF = 0x9D; //P1 secondary function control register

/*Define ADC operation const for ADC_CONTR*/
#define ADC_POWER 0x80 //ADC power control bit
#define ADC_FLAG 0x10 //ADC complete flag
#define ADC_START 0x08 //ADC start control bit
#define ADC_SPEEDL 0x00 //540 clocks
#define ADC_SPEEDL 0x20 //360 clocks
#define ADC_SPEEDH 0x40 //180 clocks
#define ADC_SPEEDHH 0x60 //90 clocks

void InitUart();
void InitADC();
void SendData(BYTE dat);
BYTE GetADCResult(BYTE ch);
void Delay(WORD n);
void ShowResult(BYTE ch);

void main()
{
    InitUart(); //Init UART, use to show ADC result
    InitADC(); //Init ADC sfr
    while (1)
    {
        ShowResult(0); //Show Channel0
        ShowResult(1); //Show Channel1
        ShowResult(2); //Show Channel2
        ShowResult(3); //Show Channel3
        ShowResult(4); //Show Channel4
        ShowResult(5); //Show Channel5
        ShowResult(6); //Show Channel6
        ShowResult(7); //Show Channel7
    }
}
```c
/*----------------------------------------------------------
Send ADC result to UART
-------------------------------------------------------------*/
void ShowResult(BYTE ch)
{
    SendData(ch);                      //Show Channel NO.
    SendData(GetADCResult(ch));       //Show ADC high 8-bit result

    //if you want show 10-bit result, uncomment next line
    //    SendData(ADC_LOW2);               //Show ADC low 2-bit result
}

/*-----------------------------------------------------------
Get ADC result
--------------------------------------------------------------*/
BYTE GetADCResult(BYTE ch)
{
    ADC_CONTR = ADC_POWER | ADC_SPEEDLL | ch | ADC_START;
    _nop_();                           //Must wait before inquiry
    _nop_();
    _nop_();
    _nop_();
    while (!(ADC_CONTR & ADC_FLAG)); //Wait complete flag
    ADC_CONTR &= ~ADC_FLAG;          //Close ADC

    return ADC_RES;                    //Return ADC result
}

/*-------------------------------------------------------------
Initial UART
----------------------------------------------------------------*/
void InitUart()
{
    SCON = 0x5a;                       //8 bit data ,no parity bit
    TMOD = 0x20;                       //T1 as 8-bit auto reload
    TH1 = TL1 = -(FOSC/12/32/BAUD);   //Set Uart baudrate
    TR1 = 1;                           //T1 start running
}

/*---------------------------------------------------------------
Initial ADC sfr
-----------------------------------------------------------------*/
void InitADC()
{
    P1ASF = 0xff;                      //Open 8 channels ADC function
    ADC_RES = 0;                       //Clear previous result
    ADC_CONTR = ADC_POWER | ADC_SPEEDLL;
    Delay(2);                          //ADC power-on and delay
}
```
Send one byte data to PC
Input: dat (UART data)
Output:

```c
void SendData(BYTE dat)
{
    while (!TI);                      //Wait for the previous data is sent
    TI = 0;                           //Clear TI flag
    SBUF = dat;                       //Send current data
}
```

Software delay function

```c
void Delay(WORD n)
{
    WORD x;
    while (n--)
    {
        x = 5000;
        while (x--);
    }
}
```
Chapter 10. Programmable Counter Array (PCA)

The Programmable Counter Array is a special 16-bit Timer that has two 16-bit capture/compare modules associated with it. Each of the modules can be programmed to operate in one of four modes: rising and/or falling edge capture (calculator of duty length for high/low pulse), software timer, high-speed output, or pulse width modulator. Each module has a pin associated with it in port 1. Module 0 is connected to pin P1.3, module 1 to pin P1.4 in STC12C5A60S2 series. While in STC12C5201AD series, module 0 is connected to pin P3.7, module 1 to pin P3.5.

The PCA timer is a common time base for all two modules and can be programmed to run at 1/12 the system clock, 1/2 the system clock, the Timer 0 overflow or the input on ECI pin(P1.2). The timer count source is determined from CPS1 and CPS0 bits in the CMOD SFR.

### 10.1 PCA Structure

![PCA Structure Diagram]

In the CMOD SFR, there are two additional bits associated with the PCA. They are CIDL which allows the PCA to stop during idle mode, and ECF which when set causes an interrupt and the PCA overflow flag CF (in the CCON SFR) to be set when the PCA timer overflows.

The CCON SFR contains the run control bit for PCA and the flags for the PCA timer and each module. To run the PCA, the CR bit (CCON.6) must be set by software; oppositely clearing bit CR will shut off PCA is shut off PCA. The CF bit (CCON.7) is set when the PCA counter overflows and an interrupt will be generated if the ECF (CMOD.0) bit in the CMOD register is set. The CF bit can only be cleared by software. There are two bits named CCF0 and CCF1 in SFR CCON. The CCF0 and CCF1 are the flags for module 0 and module 1 respectively. They are set by hardware when either a match or a capture occurs. These flags also can only be cleared by software.
10.2 SFRS for PCA

CMOD register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CIDL</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CPS2</td>
<td>CPS1</td>
<td>CPS0</td>
<td>ECF</td>
</tr>
</tbody>
</table>

CIDL : Counter Idle control. CIDL=0 programs the PCA Counter to continue functioning during idle mode. CIDL=1 programs it to be gated off during idle.

CPS2 ~ CPS0 : PCA Counter Pulse Select bits.
- 0 0 0  Internal clock, fosc/12
- 0 0 1  Internal clock, fosc/2
- 0 1 0  Timer 0 overflow
- 0 1 1  External clock at ECI/P1.2 pin
- 1 0 0  Internal clock, fosc
- 1 0 1  Internal clock, fosc/4
- 1 1 0  Internal clock, fosc/6
- 1 1 1  Internal clock, fosc/8

ECF : PCA Enable Counter Overflow interrupt. ECF=1 enables CF bit in CCON to generate an interrupt.
CCON register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>CF</td>
<td>CR</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>CCF1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCF0</td>
</tr>
</tbody>
</table>

CF : PCA Counter overflow flag. Set by hardware when the counter rolls over. CF flags an interrupt if bit ECF in CMOD is set. CF may be set by either hardware or software but can only be cleared by software.

CR : PCA Counter Run control bit. Set by software to turn the PCA counter on. Must be cleared by software to turn the PCA counter off.

CCF1 : PCA Module 1 interrupt flag. Set by hardware when a match or capture from module 1 occurs. Must be cleared by software. A match means the value of the PCA counter equals the value of the Capture/Compare register in module 1. A capture means a specific edge from CEX1 happens, so the Capture/Compare register latches the value of the PCA counter, and the CCF1 is set.

CCF0 : PCA Module 0 interrupt flag. Set by hardware when a match or capture from module 0 occurs. Must be cleared by software.

Each module in the PCA has a special function register associated with it. These registers are CCAPMn, n=0 ~1. CCAPM0 for module 0 and CCAPM1 for module 1. The register contains the bits that control the mode in which each module will operate. The ECCFn bit enables the CCFn flag in the CCON SFR to generate an interrupt when a match or compare occurs in the associated module. PWMn enables the pulse width modulation mode. The TOGn bit when set causes the CEXn output associated with the module to toggle when there is a match between the PCA counter and the module’s capture/compare register. The match bit(MATn) when set will cause the CCFn bit in the CCON register to be set when there is a match between the PCA counter and the module’s capture/compare register.

The next two bits CAPNn and CAPPn determine the edge that a capture input will be active on. The CAPNn bit enables the negative edge, and the CAPPn bit enables the positive edge. If both bits are set, both edges will be enabled and a capture will occur for either transition. The bit ECOMn when set enables the comparator function.

CCAPMn register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td>ECOMn</td>
<td>CAPPn</td>
<td>CAPNn</td>
<td>MATn</td>
<td>TOGn</td>
<td>PWMn</td>
<td>ECCFn</td>
</tr>
</tbody>
</table>

ECOMn : Enable Comparator. ECOMn=1 enables the comparator function.
CAPPn : Capture Positive, CAPPn=1 enables positive edge capture.
CAPNn : Capture Negative, CAPNn=1 enables negative edge capture.
MATn : Match. When MATn=1, a match of the PCA counter with this module’s compare/capture register causes the CCFn bit in CCON to be set.
TOGn : Toggle. When TOGn=1, a match of the PCA counter with this module’s compare/capture register causes the CEXn pin to toggle.
PWMn : Pulse Width Modulation. PWMn=1 enables the CEXn pin to be used as a pulse width modulated output.
ECCFn : Enable CCF interrupt. Enables compare/capture flag CCFn in the CCON register to generate
PCAPWMn register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>EPCnH</th>
<th>EPCnL</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>EPCnH</td>
<td>EPCnL</td>
</tr>
</tbody>
</table>

B7-B2 : Reserved
B1 (EPCnH) : Associated with CCAPnH, it is used in PCA PWM mode.
B0 (EPCnL) : Associated with CCAPnL, it is used in PCA PWM mode.

AUXR1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
<th>PCAPn</th>
<th>SPI_P4</th>
<th>S2_P4</th>
<th>GF2</th>
<th>ADRJ</th>
<th>DPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PCA_P4
0 : Default.
1 : The PCA function in P1[4:2] is switched to P4[3:1].

SPI_P4
0 : Default.
1 : The SPI function in P1[7:4] is redirected to P4[3:0].

S2_P4
0 : Default.
1 : The pin function of UART2(S2) in P1[3:2] is redirected to P4[3:2].

GF2 : General Flag. It can be used by software.

ADRJ
0 : The 10-bit conversion result of ADC is arranged as {ADC[7:0], ADCVL[1:0]}.
1 : The 10-bit conversion result is right-justified, {ADCV[1:0], ADCVL[7:0]}.

DPS
0 : Default.
1 : The secondary DPTR is switched to use.

### 10.3 PCA Module Mode

<table>
<thead>
<tr>
<th>ECOMn</th>
<th>CAPnP</th>
<th>CAPnL</th>
<th>MATn</th>
<th>TOGn</th>
<th>PWMn</th>
<th>ECFn</th>
<th>Module function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>No operation</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>16-bit capture by a positive-edge trigger on CEXn</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>16-bit capture by a negative trigger on CEXn</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>16-bit capture by a transition on CEXn</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>16-bit Software Timer</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>16-bit High Speed Output</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>8-bit PWM, no CCFn flag is set.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8-bit PWM, CCFn flag is set when PWM positive-edge transition.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8-bit PWM, CCFn flag is set when PWM negative-edge transition.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>8-bit PWM, CCFn flag is set when PWM transition.</td>
</tr>
</tbody>
</table>
PCA Capture Mode

To use one of the PCA modules in the capture mode either one or both of the CCAPM bits – CAPPn and CAPNn, for the module must be set. The external CEXn input for the module is sampled for a transition. When a valid transition occurs, the PCA hardware loads the value of the PCA counter register(CH and CL) into the module’s capture registers(CCAPnH and CCAPnL). If the CCFn bit for the module in the CCON SFR and the ECCFn bit in the CCAPMn SFR are set then an interrupt will be generated.

16-bit Software Timer Mode

The PCA modules can be used as software timers by setting both the ECOMn and MATn bits in the modules CCAPMn register. The PCA timer will be compared to the module’s capture registers and when a match occurs an interrupt will be generated if the CCFn and ECCFn bits for the module are both set.
**High Speed Output Mode**

In this mode the CEXn output (port latch) associated with the PCA module will toggle each time a match occurs between the PCA counter and the module’s capture registers. To activate this mode the TOGn,MATn,and ECOMn bits in the module’s CCAPMn SFR must be set.

**Pulse Width Modulator Mode (PWM mode)**

All of the PCA modules can be used as PWM outputs. The frequency of the output depends on the source for the PCA timer. All of the modules will have the same frequency of output because they all share the same PCA timer. The duty cycle of each module is independently variable using the module’s capture register CCAPnL and EPCnL bit in PCAPWMn register. When the value of the PCA CL SFR is less than the value in the module’s {EPCnL,CCAPnL} SFR, the output will be low. When it is equal to or greater than , the output will be high. When CL overflows from FFH to 00H, {EPCnL,CCAPnL} is reloaded with the value in {EPCnH,CCAPnH}. That allows updating the PWM without glitches. The PWMn and ECOMn bits in the module’s CCAPMn register must be set to enable the PWM mode.
10.4 Programs for PCA module extended external interrupt

There are two programs for PCA module extended external interrupt demo, one written in assembly language and the other in C language.

Assembly code listing:

```c
/*--- STC MCU International Limited---------------------------------------------*/
/*--- Mobile: (86)13922805190-----------------------------------------------------*/
/*--- Fax: 86-755-82944243---------------------------------------------------------*/
/*--- Tel: 86-755-82948412----------------------------------------------------------*/
/*--- Web: www.STCMCU.com-----------------------------------------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*-------------------------------------------------------------------------*/
```
/*Declare SFR associated with the PCA*/

CON  EQU  0D8H   ;PCA control register
CCF0 BIT  CCON.0 ;PCA module-0 interrupt flag
CCF1 BIT  CCON.1 ;PCA module-1 interrupt flag
CR  BIT  CCON.6 ;PCA timer run control bit
CF  BIT  CCON.7 ;PCA timer overflow flag
CMOD EQU  0D9H   ;PCA mode register
CL  EQU  0E9H   ;PCA base timer LOW
CH  EQU  0F9H   ;PCA base timer HIGH
CCAPM0 EQU  0DAH ;PCA module-0 mode register
CCAP0L EQU  0EAH ;PCA module-0 capture register LOW
CCAP0H EQU  0FAH ;PCA module-0 capture register HIGH
CCAPM1 EQU  0DBH ;PCA module-1 mode register
CCAP1L EQU  0EBH ;PCA module-1 capture register LOW
CCAP1H EQU  0FBH ;PCA module-1 capture register HIGH
PCA_LED BIT  P1.0 ;PCA test LED

;------------------------------------------------------------------------------------------------
ORG   0000H
LJMP  MAIN

ORG   003BH

PCA_ISR:
CLR   CCF0 ;Clear interrupt flag
CPL   PCA_LED ;toggle the test pin while CEX0(P1.3) have a falling edge
RETI

;------------------------------------------------------------------------------------------------
ORG   0100

MAIN:
MOV   CCON, #0 ;Initial PCA control register
;PCA timer stop running
;Clear CF flag
;Clear all module interrupt flag
CLR   A
MOV   CL, A ;Reset PCA base timer
MOV   CH, A ;
MOV   CMOD, #00H ;Set PCA timer clock source as Fosc/12
;Disable PCA timer overflow interrupt
MOV   CCAPM0, #11H ;PCA module-0 capture by a falling edge on CEX0(P1.3)
;and enable PCA interrupt
;MOV   CCAPM0, #31H ;PCA module-0 capture by a transition (falling/rising edge)
on CEX0(P1.3) and enable PCA interrupt

;------------------------------------------------------------------------------------------------
SETB   CR ;PCA timer start run

SETB   EA

SJMP   $ ;-----------------------------------------
END
C code listing:

/*----------------------------------------*/
/* --- STC MCU International Limited ----*/
/* --- STC 1T Series MCU PCA module Extended external interrupt ----*/
/* --- Mobile: (86)13922805190 -----------------------------------------------*/
/* --- Fax: 86-755-82944243 ---------------------------------------------------*/
/* --- Tel: 86-755-82948412 ----------------------------------------------------*/
/* --- Web: www.STCMCU.com -----------------------------------------------------*/
/* If you want to use the program or the program referenced in the article, please specify in which data and procedures from STC */
/*--------------------------------------------------------------------------------*/

#include "reg51.h"
#include "intrins.h"

typedef unsigned char BYTE;
typedef unsigned int WORD;

/*Declare SFR associated with the PCA */

sfr CCON = 0xD8; //PCA control register
sbit CCF0 = CCON^0; //PCA module-0 interrupt flag
sbit CCF1 = CCON^1; //PCA module-1 interrupt flag
sbit CR = CCON^6; //PCA timer run control bit
sbit CF = CCON^7; //PCA timer overflow flag
sfr CMOD = 0xD9; //PCA mode register
sfr CL = 0xE9; //PCA base timer LOW
sfr CH = 0xF9; //PCA base timer HIGH
sfr CCAPM0 = 0xDA; //PCA module-0 mode register
sfr CCAPOL = 0xEA; //PCA module-0 capture register LOW
sfr CCAP0H = 0xFA; //PCA module-0 capture register HIGH
sfr CCAPM1 = 0xDB; //PCA module-1 mode register
sfr CCAP1L = 0xEB; //PCA module-1 capture register LOW
sfr CCAP1H = 0xFB; //PCA module-1 capture register HIGH
sfr PCAPWM0 = 0xf2;
sfr PCAPWM1 = 0xf3;

sbit PCA_LED = P1^0; //PCA test LED

void PCA_isr() interrupt 7 using 1 {
    CCF0 = 0; //Clear interrupt flag
    PCA_LED = !PCA_LED; //toggle the test pin while CEX0(P1.3) have a falling edge
}
void main()
{
    CCON = 0;                        //Initial PCA control register
    //PCA timer stop running
    //Clear CF flag
    //Clear all module interrupt flag
    CL = 0;                           //Reset PCA base timer
    CH = 0;
    CMOD = 0x00;                      //Set PCA timer clock source as Fosc/12
    //Disable PCA timer overflow interrupt
    CCAPM0 = 0x11;                 //PCA module-0 capture by a negative trigger on CEX0(P1.3)
    //and enable PCA interrupt
    CR = 1;                           //PCA timer start run
    EA = 1;

    while (1);
}

10.5 Example Programs for PCA module acted as 16-bit Timer

There are two programs for PCA module acted as 16-bit Timer demo, one written in assembly language and the other in C language.

Assembly code listing:
; *-----------------------------------------------------------------------------------------------*/
; /* --- STC MCU International Limited ---------------------------------------------------*/
; /* --- STC 1T Series MCU PCA module acted as 16-bit Timer Demo ------------------------*/
; /* --- Mobile: (86)13922805190 --------------------------------------------------------*/
; /* --- Fax: 86-755-82944243 -----------------------------------------------------------*/
; /* --- Tel: 86-755-82948412 --------------------------------------------------------------*/
; /* --- Web: www.STCMCU.com -------------------------------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; *-----------------------------------------------------------------------------------------------*/

T100Hz EQU 3C00H                ;(18432000 / 12 / 100)

; /* Declare SFR associated with the PCA */
    CCON EQU 0D8H ;PCA control register
    CCF0 BIT CCON.0 ;PCA module-0 interrupt flag
    CCF1 BIT CCON.1 ;PCA module-1 interrupt flag
    CR BIT CCON.6 ;PCA timer run control bit
    CF BIT CCON.7 ;PCA timer overflow flag
    CMOD EQU 0D9H ;PCA mode register
    CL EQU 0E9H ;PCA base timer LOW
    CH EQU 0F9H ;PCA base timer HIGH
    CCAPM0 EQU 0DAH ;PCA module-0 mode register
CCAP0L EQU 0EAH ; PCA module-0 capture register LOW
CCAP0H EQU 0FAH ; PCA module-0 capture register HIGH
CCAPM1 EQU 0DBH ; PCA module-1 mode register
CCAP1L EQU 0EBH ; PCA module-1 capture register LOW
CCAP1H EQU 0FBH ; PCA module-1 capture register HIGH

PCA_LED BIT P1.0 ; PCA test LED
CNT EQU 20H

;------------------------------------------------------------------------
ORG 0000H
LJMP MAIN

ORG 003BH
LJMP PCA_ISR

;------------------------------------------------------------------------
ORG 0100H
MAIN:

MOV SP, #3FH ; Initial stack point
MOV CCON, #0 ; Initial PCA control register

; PCA timer stop running
CLR A ; Clear CF flag
MOV CL, A ; Clear all module interrupt flag
MOV CH, A ;
MOV CMOD, #00H ; Set PCA timer clock source as Fosc/12

;-----------------------------------------------------------------------------
MOV CCAP0L, #LOW T100Hz ; Initial PCA module-0
MOV CCAP0H, #HIGH T100Hz ; PCA module-0 work in 16-bit timer mode
MOV CCAPM0, #49H ; and enable PCA interrupt

;-------------------------------------------------------------------------------
SETB CR ; PCA timer start run

SETB EA
MOV CNT, #100
SJMP $ ;---------------------------------------------------------------------------------

PCA_ISR:

PUSH PSW ; Clear interrupt flag
PUSH ACC
CLR CCF0
MOV A, CCAP0L
ADD A, #LOW T100Hz ; Update compare value
MOV CCAP0L, A
MOV A, CCAP0H
ADDC A, #HIGH T100Hz
MOV CCAP0H, A
DJNZ CNT, PCA_ISR_EXIT ;count 100 times
MOV CNT, #100
CPL PCA_LED ;Flash once per second

PCÆ_ISR_EXIT:
POP ACC
POP PSW
RETI

END

C code listing:

/*--------------------------*/
/* --- STC MCU International Limited -------------------------------*/
/* --- STC 1T Series MCU PCA module acted as 16-bit Timer Demo ------*/
/* --- Mobile: (86)13922805190 --------------------------------------*/
/* --- Fax: 86-755-82944243 ------------------------------------------*/
/* --- Tel: 86-755-82948412 -------------------------------------------*/
/* --- Web: www.STCMCU.com ------------------------------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*-----------------------------------------------------------------*/

#include "reg51.h"
#include "intrins.h"
#define FOSC 18432000L
#define T100Hz (FOSC / 12 / 100)
typedef unsigned char BYTE;
typedef unsigned int WORD;

/*Declare SFR associated with the PCA */
sfr CCON = 0xD8; //PCA control register
sbit CCF0 = CCON^0; //PCA module-0 interrupt flag
sbit CCF1 = CCON^1; //PCA module-1 interrupt flag
sbit CR = CCON^6; //PCA timer run control bit
sbit CF = CCON^7; //PCA timer overflow flag
sfr CMOD = 0xD9; //PCA mode register
sfr CL = 0xE9; //PCA base timer LOW
sfr CH = 0xF9; //PCA base timer HIGH
sfr CCAPM0 = 0xDA; //PCA module-0 mode register
sfr CCAP0L = 0xEA; //PCA module-0 capture register LOW
sfr CCAP0H = 0xFA; //PCA module-0 capture register HIGH
sfr CCAPM1 = 0xFB; //PCA module-1 mode register
sfr CCAP1L = 0xEB; //PCA module-1 capture register LOW
sfr CCAP1H = 0xFB; //PCA module-1 capture register HIGH
sfr PCAPWM0=0xf2;
sfr PCAPWM1=0xf3;
sbit PCA_LED = P1^0;  //PCA test LED

BYTE cnt;
WORD value;

void PCA_isr() interrupt 7 using 1
{
    CCF0 = 0;                         //Clear interrupt flag
    CCAP0L = value;
    CCAP0H = value >> 8;             //Update compare value
    value += T100Hz;
    if (cnt-- == 0)
    {
        cnt = 100;                   //Count 100 times
        PCA_LED = !PCA_LED;   //Flash once per second
    }
}

void main()
{
    CCON = 0;                         //Initial PCA control register
                                        // PCA timer stop running
                                        // Clear CF flag
                                        // Clear all module interrupt flag
    CL = 0;                           //Reset PCA base timer
    CH = 0;
    CMOD = 0x00;                      //Set PCA timer clock source as Fosc/12
                                        // Disable PCA timer overflow interrupt
    value = T100Hz;
    CCAP0L = value;
    CCAP0H = value >> 8;             //Initial PCA module-0
    value += T100Hz;
    CCAPM0 = 0x49;                    //PCA module-0 work in 16-bit timer mode
                                        // and enable PCA interrupt
    CR = 1;                          //PCA timer start run
    EA = 1;
    cnt = 0;

    while (1);
}
10.6 Programs for PCA module as 16-bit High Speed Output

There are two programs for PCA module as 16-bit High Speed Output, one written in assembly language and the other in C language.

Assembly code listing:

```assembly
T100KHz  EQU  2EH           ;(18432000 / 4 / 100000)

Declare SFR associated with the PCA:

CCON    EQU  0D8H             ;PCA control register
CCF0    BIT  CCON.0           ;PCA module-0 interrupt flag
CCF1    BIT  CCON.1           ;PCA module-1 interrupt flag
CR      BIT  CCON.6           ;PCA timer run control bit
CF      BIT  CCON.7           ;PCA timer overflow flag
CMOD    EQU  0D9H             ;PCA mode register
CL      EQU  0E9H             ;PCA base timer LOW
CH      EQU  0F9H             ;PCA base timer HIGH
CCAPM0  EQU  0DAH             ;PCA module-0 mode register
CCAP0L  EQU  0EAH             ;PCA module-0 capture register LOW
CCAP0H  EQU  0FAH             ;PCA module-0 capture register HIGH
CCAPM1  EQU  0DBH             ;PCA module-1 mode register
CCAP1L  EQU  0EBH             ;PCA module-1 capture register LOW
CCAP1H  EQU  0FBH             ;PCA module-1 capture register HIGH

ORG     0000H
LJMP    MAIN

ORG     003BH

PCA_ISR:

PUSH    PSW
PUSH    ACC
CLR     CCF0                    ;Clear interrupt flag
MOV     A, CCAP0L               ;Update compare value
ADD     A, #T100KHz
MOV     CCAP0L,A
CLR     A
ADDC    A, CCAP0H
```
MOV CCAP0H, A

PCA_ISR_EXIT:
POP ACC
POP PSW
RETI

;-----------------------------------------------------------------------
ORG 0100H
 MAIN:
MOV CCON, #0 ;Initial PCA control register
 ;PCA timer stop running
 ;Clear CF flag
 ;Clear all module interrupt flag
CLR A
MOV CL, A ;Reset PCA base timer
MOV CH, A ;
MOV CMOD, #02H ;Set PCA timer clock source as Fosc/2
 ;Disable PCA timer overflow interrupt

;-----------------------------------------------------------------------
MOV CCAP0L, #T100KHz ;P1.3 output 100KHz square wave
MOV CCAP0H, #0 ;Initial PCA module-0
MOV CCAPM0, #4dH ;PCA module-0 work in 16-bit timer mode and enable
 ;PCA interrupt, toggle the output pin CEX0(P1.3)
 ;-----------------------------------------------------------------------
 SETB CR ;PCA timer start run
SETB EA
SJMP $ ;-----------------------------------------------------------------------
END

C code listing:
;/*--------------------------------------------------------------------------------------*/
;/* --- STC MCU International Limited -----------------------------------------*/
;/* --- STC 1T Series MCU PCA module as 16-bit High Speed Output ----*/
;/* --- Mobile: (86)13922805190 ------------------------------------------*/
;/* --- Fax: 86-755-82944243 --------------------------------------------------*/
;/* --- Tel: 86-755-82948412 ----------------------------------------------------*/
;/* --- Web: www.STCMCU.com ----------------------------------------------------*/
;/* If you want to use the program or the program referenced in the */
;/* article, please specify in which data and procedures from STC */
;/*---------------------------------------------------------------------*/

#include "reg51.h"
#include "intrins.h"
#define FOSC 18432000L
#define T100KHz (FOSC / 4 / 100000)
typedef unsigned char BYTE;
typedef unsigned int WORD;
/*Declare SFR associated with the PCA */
sfr  CCON = 0xD8;             //PCA control register
sbit  CCF0 = CCON^0;           //PCA module-0 interrupt flag
sbit  CCF1 = CCON^1;           //PCA module-1 interrupt flag
sbit  CR = CCON^6;           //PCA timer run control bit
sbit  CF     = CCON^7;           //PCA timer overflow flag
sfr  CMOD = 0xD9;             //PCA mode register
sfr  CL           = 0xE9;             //PCA base timer LOW
sfr  CH          = 0xF9;             //PCA base timer HIGH
sfr  CCAPM0=   0xDA;             //PCA module-0 mode register
sfr  CCAPOL =   0xEA;             //PCA module-0 capture register LOW
sfr  CCAP0H =   0xFA;             //PCA module-0 capture register HIGH
sfr  CCAPM1=   0xDB;             //PCA module-1 mode register
sfr  CCAP1L  =   0xEB;             //PCA module-1 capture register LOW
sfr  CCAP1H =   0xFB;             //PCA module-1 capture register HIGH
sfr  PCAPWM0=0xf2;
sfr  PCAPWM1=0xf3;
sbit  PCA_LED=   P1^0;             //PCA test LED
BYTE  cnt;
WORD  value;
void PCA_isr() interrupt 7 using 1
{
    CCF0 = 0;                          //Clear interrupt flag
    CCAP0L = value;
    CCAP0H = value >> 8;              //Update compare value
    value += T100KHz;
}
void main()
{
    CCON = 0;                          //Initial PCA control register
    //PCA timer stop running
    //Clear CF flag
    //Clear all module interrupt flag
    CL = 0;                            //Reset PCA base timer
    CH = 0;
    CMOD = 0x02;                       //Set PCA timer clock source as Fosc/2
    //Disable PCA timer overflow interrupt
    value = T100KHz;
    CCAPOL = value;
    CCAP0H = value >> 8;              //Initial PCA module-0
    value += T100KHz;
    CCAPM0 = 0x4d;
    //PCA module-0 work in 16-bit timer mode and
    //enable PCA interrupt, toggle the output pin CEX0(P1.3)
    CR = 1;                            //PCA timer start run
    EA = 1;
cnt = 0;
while (1);
10.7 Example Programs for PCA module as PWM Output

Assembly code listing:

*--------------------------------------------------------------------------*/
; /* --- STC MCU International Limited --------------------------------------*/
; /* --- STC 1T Series MCU PCA module output PWM wave Demo -----------------*/
; /* --- Mobile: (86)13922805190 --------------------------------------------*/
; /* --- Fax: 86-755-82944243 -----------------------------------------------*/
; /* --- Tel: 86-755-82948412 ------------------------------------------------*/
; /* --- Web: www.STCMCU.com -----------------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; /*--------------------------------------------------------------------------*/

; //Declare SFR associated with the PCA */
CCON   EQU  0D8H             ;PCA control register
CCF0   BIT  CCON.0           ;PCA module-0 interrupt flag
CCF1   BIT  CCON.1           ;PCA module-1 interrupt flag
CR     BIT  CCON.6           ;PCA timer run control bit
CF     BIT  CCON.7           ;PCA timer overflow flag
CMOD   EQU  0D9H             ;PCA mode register
CL     EQU  0E9H             ;PCA base timer LOW
CH     EQU  0F9H             ;PCA base timer HIGH
CCAPM0 EQU  0DAH             ;PCA module-0 mode register
CCAP0L  EQU  0EAH            ;PCA module-0 capture register LOW
CCAP0H  EQU  0FAH            ;PCA module-0 capture register HIGH
CCAPM1  EQU  0DBH            ;PCA module-1 mode register
CCAP1L  EQU  0EBH            ;PCA module-1 capture register LOW
CCAP1H  EQU  0FBH            ;PCA module-1 capture register HIGH

ORG    0000H
LJMP   MAIN

ORG    0100H

MAIN:

MOV    CCON, #0             ;Initial PCA control register
       ;PCA timer stop running
       ;Clear CF flag
       ;Clear all module interrupt flag
       ;Reset PCA base timer
CLR    A
MOV    CL, A
MOV    CH, A
MOV    CMOD, #02H          ;Set PCA timer clock source as Fosc/2
       ;Disable PCA timer overflow interrupt
MOV    A, #080H            ;PWM0 port output 50% duty cycle square wave
MOV    CCAP0H, A
MOV    CCAP0L, A
MOV    CCAPM0, #42H        ;PCA module-0 work in 8-bit PWM mode
       ;and no PCA interrupt
Mov A, #0C0h ;PWM1 port output 25% duty cycle square wave
Mov CCAP1H,A ;
Mov CCAP1L,A ;
Mov CCAPM1,#42h ;PCA module-1 work in 8-bit PWM mode
;and no PCA interrupt

Setb CR ;PCA timer start run
Sjmp $

C code listing:
*------------------------------------------------------------------------------------------*/
/* --- STC MCU International Limited ------------------------------------------------------*/
/* --- STC 1T Series MCU PCA module output PWM wave Demo --------------------------------*/
/* --- Mobile: (86)13922805190 --------------------------------------------------------------*/
/* --- Fax: 86-755-82944243 ------------------------------------------------------------------*/
/* --- Tel: 86-755-82948412 --------------------------------------------------------------------*/
/* --- Web: www.STCMCU.com -------------------------------------------------------------------*/
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*------------------------------------------------------------------------------------------*/

#include "reg51.h"
#include "intrins.h"

define FOSC 18432000L

typedef unsigned char BYTE;
typedef unsigned int WORD;

/*Declare SFR associated with the PCA */
sfr CCON = 0xD8;    //PCA control register
sbit CCF0 = CCON^0; //PCA module-0 interrupt flag
sbit CCF1 = CCON^1; //PCA module-1 interrupt flag
sbit CR = CCON^6;  //PCA timer run control bit
sbit CF = CCON^7;  //PCA timer overflow flag
sfr CMOD = 0xD9;   //PCA mode register
sfr CL = 0xE9;     //PCA base timer LOW
sfr CH = 0xF9;     //PCA base timer HIGH
sfr CCAPM0= 0xDA;  //PCA module-0 mode register
sfr CCAPOL = 0xEA; //PCA module-0 capture register LOW
sfr CCAPOH = 0xFA; //PCA module-0 capture register HIGH
sfr CCAPM1= 0xDB;  //PCA module-1 mode register
sfr CCAP1L = 0xEB; //PCA module-1 capture register LOW
sfr CCAP1H = 0xFB; //PCA module-1 capture register HIGH
sfr PCAPWM0=0xf2;
sfr PCAPWM1=0xf3;
void main()
{
    CCON = 0;                           //Initial PCA control register
    //PCA timer stop running
    //Clear CF flag
    //Clear all module interrupt flag
    CL = 0;                           //Reset PCA base timer
    CH = 0;
    CMOD = 0x02;                      //Set PCA timer clock source as Fosc/2
    //Disable PCA timer overflow interrupt
    CCAP0H = CCAP0L = 0x80;          //PWM0 port output 50% duty cycle square wave
    CCAPM0 = 0x42;                    //PCA module-0 work in 8-bit PWM mode
    //and no PCA interrupt
    CCAP1H = CCAP1L = 0xff;          //PWM1 port output 0% duty cycle square wave
    PCAPWM1 = 0x03;
    CCAPM1 = 0x42;                    //PCA module-1 work in 8-bit PWM mode
    //and no PCA interrupt
    CR = 1;                           //PCA timer start run
    while (1);
}
10.8 PCA clock base on Timer1 overflow rate

; *--------------------------------------------------------------------------;
; /* --- STC MCU International Limited -----------------------------------*/
; /* --- STC 1T Series achieve adjustable frequency PWM output ----------*/
; /* --- Mobile: (86)13922805190 ------------------------------------------*/
; /* --- Fax: 86-755-82944243 ---------------------------------------------*/
; /* --- Tel: 86-755-82948412 ---------------------------------------------*/
; /*--- Web: www.STCMCU.com ---------------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; *--------------------------------------------------------------------------*/

;/*Declare SFR associated with the ADC */
IPH       EQU 0B7H ;Interrupt priority control register high byte
CCON      EQU 0D8H ;PCA control register
CCF0      BIT CCON.0 ;PCA module-0 interrupt flag
CCF1      BIT CCON.1 ;PCA module-1 interrupt flag
CR        BIT CCON.6 ;PCA timer run control bit
CF        BIT CCON.7 ;PCA timer overflow flag
CMOD      EQU 0D9H ;PCA mode register
CL        EQU 0E9H ;PCA base timer LOW
CH        EQU 0F9H ;PCA base timer HIGH
CCAPM0    EQU 0DAH ;PCA module-0 mode register
CCAP0L    EQU 0EAH ;PCA module-0 capture register LOW
CCAP0H    EQU 0FAH ;PCA module-0 capture register HIGH
CCAPM1    EQU 0DBH ;PCA module-1 mode register
CCAP1L    EQU 0EBH ;PCA module-1 capture register LOW
CCAP1H    EQU 0FBH ;PCA module-1 capture register HIGH

;/*Define working LED */
LED_MCU_START  EQU P1.7
LED_5ms_Flashing EQU P1.6
LED_1S_Flashing EQU P1.5

Channel_5mS_H  EQU 01H ;PCA module-1 5ms counter high byte @ 18.432MHz
Channel_5mS_L  EQU 00H ;PCA module-1 5ms counter low byte @ 18.432MHz
Timer0_Reload_1 EQU 0F6H ;Timer0 auto reload value (-10)
Timer0_Reload_2 EQU 0ECH ;Timer0 auto reload value (-20)
PWM_WIDTH     EQU 0FFH ;low duty
Counter       EQU 030H ;counter value

;--------------------------------------------------------------------------
ORG 0000H
LJMP MAIN
ORG 003BH
LJMP PCA_interrupt
;--------------------------------------------------------------------------
ORG 0050H

MAIN:
CLR LED_MCU_START ;Turn on MCU working LED
MOV SP,#7FH
MOV Counter,#0 ;initial Counter var
ACALL PAC_Initial ;initial PCA
ACALL Timer0_Initial ;Initial Timer0

MAIN_Loop:
;-------------------------------
MOV TH0,#Timer0_Reload_1 ;Set Timer0 overload rate 1
MOV TL0,#Timer0_Reload_1
MOV A,#PWM_WIDTH ;setting duty
MOV CCAP0H,A
ACALL delay
MOV TH0,#Timer0_Reload_2 ;Set Timer0 overload rate 2
MOV TL0,#Timer0_Reload_2
ACALL delay

;-------------------------------
MOV TH0,#Timer0_Reload_1 ;Set Timer0 overload rate 1
MOV TL0,#Timer0_Reload_1
MOV A,#PWM_WIDTH
ACALL RL_A ;change duty
ACALL RL_A
MOV CCAP0H,A
ACALL delay
MOV TH0,#Timer0_Reload_2 ;Set Timer0 overload rate 2
MOV TL0,#Timer0_Reload_2
ACALL delay

;-------------------------------
MOV TH0,#Timer0_Reload_1 ;Set Timer0 overload rate 1
MOV TL0,#Timer0_Reload_1
MOV A,#PWM_WIDTH
ACALL RL_A ;change duty
ACALL RL_A
ACALL RL_A
ACALL RL_A
MOV CCAP0H,A
ACALL delay
MOV TH0,#Timer0_Reload_2 ;Set Timer0 overload rate 2
MOV TL0,#Timer0_Reload_2
ACALL delay

;-------------------------------
SJMP MAIN_Loop

;-----------------------------------------
RL_A:
CLR C
RRC A
RET
;---------------------------------------------------------------------------
Timer0_Initial:
    MOV  TMOD,#02H   ;8-bit auto-reload
    MOV  TH0,#Timer0_Reload_1
    MOV  TL0,#Timer0_Reload_1
    SETB  TR0        ;strat run
    RET

;---------------------------------------------------------------------------
PCA_Initial:
    MOV  CMOD,#10000100B ;PCA timer base on Timer0
    MOV  CCON,#00H    ;PCA stop count
    MOV  CL,#0        ;initial PCA counter
    MOV  CH,#0
    MOV  CCAPM0,#42H  ;PCA module-0 as 8-bit PWM
    MOV  PCA_PWM0,#0  ;PWM mode 9\textsuperscript{th} bit
    MOV  PCA_PWM0,#03H ;PWM will keep low level
    MOV  CCAP1L,#Channel_5mS_L ;initial PCA module-1
    MOV  CCAP1H,#Channel_5mS_H
    MOV  CCAPM1,#49H  ;PCA module-1 as 16-bit timer
    SETB  EA
    SETB  CR          ;PCA counter start running
    RET

;---------------------------------------------------------------------------
PCA_Interrupt:
    PUSH  ACC
    PUSH  PSW
    CPL   LED_5mS_Flashing       ;Flashing once per 5ms
    MOV   A,#Channel_5mS_L
    ADD   A,CCAP1L
    MOV   CCAP1L,A
    MOV   A,#Channel_5mS_H
    ADDC  A,CCAP1H
    MOV   CCAP1H,A
    CLR   CCF1                ;Clear PCA module-1 flag
    INC   Counter
    MOV   A,Counter
    CLR   C
    SUBB  A,#100      ;Count 100 times
    JC    PCA_Interrupt_Exit
    MOV   Counter,#0
    CPL   LED_1S,Flash
PCA_Interrupt_Exit:
    POP   PSW
    POP   ACC
    RETI

;---------------------------------------------------------------------------
10.9 Using PWM achieve D/A Conversion function reference circuit
Chapter 11 Serial Peripheral Interface (SPI)

STC12C5A60S2 provides another high-speed serial communication interface, the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3Mbit/s can be supported in either Master or Slave mode under the SYSclk=12MHz. Two status flags are provided to signal the transfer completion and write-collision occurrence.

11.1 SPI Structure

The SPI interface has three pins implementing the SPI functionality: SCLK(P1.7), MISO(P1.6), MOSI(P1.5). An extra pin SS(P1.4) is designed to configure the SPI to run under Master or Slave mode. SCLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI(Master Out Slave In) pin and flows from slave to master on MISO(Master In Slave Out) pin. The SCLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN(SPCTL.6)=0, these pins are configured as general-purposed I/O port(P1.4 ~ P1.7).

SS is the slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its SS pin to determine whether it is selected. But if SPEN=0 or SSIG(SPCTL.7) bit is 1, the SS pin is ignored. Note that even if the SPI is configured as a master(MSTR/SPCTL.4=1), it can still be converted to a slave by driving the SS pin low. When the conversion happened, the SPIF bit(SPSTAT.7) will be set.
Two devices with SPI interface communicate with each other via one synchronous clock signal, one input data signal, and one output data signal. There are two concerns the user should take care, one of them is latching data on the negative edge or positive edge of the clock signal which named polarity, the other is keeping the clock signal low or high while the device idle which named phase. Permuting those states from polarity and phase, there could be four modes formed, they are SPI-MODE-0, SPI-MODE-1, SPI-MODE-2, SPI-MODE-3. Many device declares that they meet SPI mechanism, but few of them are adaptive to all four modes. The STC12C5A60S2 series are flexible to be configured to communicate to another device with MODE-0, MODE-1, MODE-2 or MODE-3 SPI, and play part of Master and Slave.

11.2 Special Function Registers for SPI

SPCTL register (SPI Control register)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SSIG</td>
<td>SPEN</td>
<td>DORD</td>
<td>MSTR</td>
<td>CPOL</td>
<td>CPHA</td>
<td>SPR1</td>
<td>SPR0</td>
</tr>
</tbody>
</table>

SSIG : SS is ignored. If SSIG=1, MSTR decides whether the device is a master or slave. If SSIG=0, the SS pin decides whether the device is master or slave.

SPEN : SPI enable. If SPEN=0, the SPI interface is disabled and all SPI pins will be general-purpose I/O ports. If SPEN=1, the SPI is enabled.

DORD : SPI data order.
  1 : The LSB of the data word is transmitted first.
  0 : The MSB of the data word is transmitted first.

MSTR : Master/Slave mode select. If MSTR=0, set the SPI to play as Slave part. If MSTR=1, set the SPI to play as Master part.

CPOL : SPI clock polarity select.
  1 : SPICLK is high when idle. The leading edge of SPICLK is the falling edge and the trailing edge is the rising edge.
  0 : SPICLK is low when idle. The leading edge of SPICLK is the rising edge and the trailing edge is the falling edge.

CPHA : SPI clock phase select.
  1 : Data is driven on the leading edge of SPICLK, and is sampled on the trailing edge.
  0 : Data is driven when SS pin is low(SSIG=0) and changes on the trailing edge of SPICLK. Data is sampled on the leading edge of SPICLK. (Note : If SSIG=1, CPHA must not be 0, otherwise the operation is undefined)

SPR1-SPR0 : SPI clock rate select (when in master mode)
  00 : Set the clock rate of the SPI as SYSclk/4
  01 : Set the clock rate of the SPI as SYSclk/16
  10 : Set the clock rate of the SPI as SYSclk/64
  11 : Set the clock rate of the SPI as SYSclk/128

When CPHA equals 0, SSIG must be 0 and SS pin must be negated and reasserted between each successive serial byte transfer. If the SPDAT register is written while SS is active(0), a write collision error results and WCOL is set.

When CPHA equals 1, SSIG may be 0 or 1. If SSIG=0, the SS pin may remain active low between successive transfers(can be tied low at any times). This format is sometimes preferred for use in systems having a signle fixed master and a single slave configuration.
SPDAT (SPI Data) register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The SFR SPDAT holds the data to be transmitted or the data received.

SPSTAT register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>SPIF</td>
<td>WCOL</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

SPIF : SPI transfer completion flag. When a serial transfer finishes, the SPIF bit is set and an interrupt is generated if both the ESPI (IE.6) bit and the EA (IE.7) bit are set. If SS is an input and is driven low when SPI is in master mode with SSIG = 0, SPIF will also be set to signal the “mode change”. The SPIF is cleared in software by “writing 1 to this bit”.

WCOL : SPI write collision flag. The WCOL bit is set if the SPI data register, SPDAT, is written during a data transfer. The WCOL flag is cleared in software by “writing 1 to this bit”.

AUXR1 register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td>PCA_P4</td>
<td>SPI_P4</td>
<td>S2_P4</td>
<td>GF2</td>
<td>ADRJ</td>
<td>-</td>
<td>DPS</td>
</tr>
</tbody>
</table>

SPI_P4

0 : Default.
1 : The SPI function in P1[7:4] is redirected to P4[3:0].

Auxiliary Interrupt Enable register (IE2)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>ESPI</td>
</tr>
</tbody>
</table>

ESPI : When set, enables SPI interrupt.

Interrupt Priority Low register 2 (IP2)

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>PSPI</td>
</tr>
</tbody>
</table>

PSPI : SPI interrupt priority bit.

11.3 SPI Data Communication

Table: SPI master and slave selection

<table>
<thead>
<tr>
<th>SPEN</th>
<th>SSIG</th>
<th>SS</th>
<th>MSTR</th>
<th>Mode</th>
<th>MISO</th>
<th>MOSI</th>
<th>SPICLK</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>SPI disable</td>
<td>GPI/O</td>
<td>GPI/O</td>
<td>GPI/O</td>
<td>SPI is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Selected slave</td>
<td>output</td>
<td>input</td>
<td>input</td>
<td>Selected as slave</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Unselected slave</td>
<td>Hi-Z</td>
<td>input</td>
<td>input</td>
<td>Not selected.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1-&gt;0</td>
<td>slave</td>
<td>output</td>
<td>input</td>
<td>input</td>
<td>Convert from Master to Slave</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Master</td>
<td>input</td>
<td>output</td>
<td>output</td>
<td>SPICLK depends on CPOL</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
<td>slave</td>
<td>output</td>
<td>input</td>
<td>input</td>
<td>Slave</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>Master</td>
<td>input</td>
<td>output</td>
<td>output</td>
<td>Master</td>
</tr>
</tbody>
</table>
Typical Connection

**SPI single master single slave configuration**

**SPI dual device configuration, where either can be a master or slave**

**SPI single master multiple slaves configuration**
Communication

In SPI, transfers are always initiated by the master. If the SPI is enabled (SPEN=1) and selected as master, any instruction that use SPI data register SPDAT as the destination will starts the SPI clock generator and a data transfer. The data will start to appear on MOSI about one half SPI bit-time to one SPI bit-time after it. Before starting the transfer, the master may select a slave by driving the SS pin of the corresponding device low. Data written to the SPDAT register of the master shifted out of MOSI pin of the master to the MOSI pin of the slave. And at the same time the data in SPDAT register of the selected slave is shifted out of MISO pin to the MISO pin of the master. During one byte transfer, data in the master and in the slave is interchanged. After shifting one byte, the transfer completion flag (SPIF) is set and an interrupt will be created if the SPI interrupt is enabled.

If SPEN=1, SSIG=0, SS pin=1 and MSTR=1, the SPI is enabled in master mode. Before the instruction that use SPDAT as the destination register, the master is in idle state and can be selected as slave device by any other master drives the idle master SS pin low. Once this happened, MSTR bit of the idle master is cleared by hardware and changes its state a selected slave. User software should always check the MSTR bit. If this bit is cleared by the mode change of SS pin and the user wants to continue to use the SPI as a master later, the user must set the MSTR bit again, otherwise it will always stay in slave mode.

The SPI is single buffered in transmit direction and double buffered in receive direction. New data for transmission can not be written to the shift register until the previous transaction is complete. The WCOL bit is set to signal data collision when the data register is written during transaction. In this case, the data currently being transmitted will continue to be transmitted, but the new data which causing the collision will be lost. For receiving data, received data is transferred into a internal parallel read data buffer so that the shift register is free to accept a second byte. However, the received byte must be read from the data register (SPDAT) before the next byte has been completely transferred. Otherwise the previous byte is lost. WCOL can be cleared in software by “writing 1 to the bit”.

Typical Timing Diagram

![Typical Timing Diagram](image)

SPI slave transfer format with CPHA=0
*When P4SPI bit in AUXR1 register is set, the function of SPI is redirected from P3[7:4] to P4[7:4] pin by pin.*
11.4 SPI Function Demo(Single Master Single Slave)(ASM)

The following program, written in assembly language, tests SPI function and applies to SPI single master single slave configuration.

```assembly
; *-------------------------------------------------------------------
; /* --- STC MCU International Limited ---------------------------*/
; /* --- STC 1T Series MCU SPI Demo(1 master and 1 slave) ----------*/
; /* --- Mobile: (86)13922805190 --------------------------------*/
; /* --- Fax: 86-755-82944243 -------------------------------------*/
; /* --- Tel: 86-755-82948412 --------------------------------------*/
; /* --- Web: www.STCMCU.com --------------------------------------*/
; /* If you want to use the program or the program referenced in the */
; /* article, please specify in which data and procedures from STC */
; /* *----------------------------------------------------------------

#define  MASTER                    //define: master undefine: slave

AUXR     DATA     08EH              ; Auxiliary register
SPSTAT   DATA     0CDH              ; SPI status register
SPIF     EQU      080H              ; SPSTAT.7
WCOL     EQU      040H              ; SPSTAT.6
SPCTL    DATA     0CEH              ; SPI control register
SSIG     EQU      080H              ; SPCTL.7
SPEN     EQU      040H              ; SPCTL.6
DORD     EQU      020H              ; SPCTL.5
MSTR     EQU      010H              ; SPCTL.4
CPOL     EQU      008H              ; SPCTL.3
CPHA     EQU      004H              ; SPCTL.2
SPDH    EQU      000H               ; CPU_CLK/4
SPD     EQU      001H               ; CPU_CLK/16
SPDL    EQU      002H               ; CPU_CLK/64
SPDLL   EQU      003H               ; CPU_CLK/128
SPDAT   DATA     0CFH               ; SPI data register
SPISS    BIT    P1.3               ; SPI slave select, connect to slave' SS(P1.4) pin

; ///////////////////////////////////////////////////////////////////////////
ORG      0000H
LJMP     RESET
ORG      0100H
RESET:
   LCALL    INIT_UART           ; initial UART
   LCALL    INIT_SPI           ; initial SPI
```

STC MCU Limited

website: www.STCMCU.com
MAIN:
#ifdef MASTER
       //for master (receive UART data from PC and send it to slave, in the meantime
       LCALL RECV_UART ; receive SPI data from slave and send it to PC)
       LCALL SPI_SWAP
       LCALL SEND_UART
#else
       //for slave (receive SPI data from master and
       LCALL SPI_SWAP ; send previous SPI data to master)
#endif
SJMP MAIN

;/////////////////////////////////////////////////////////////////////////////////////

INIT_UART:
    MOV SCON, #5AH ; set UART mode as 8-bit variable baudrate
    MOV TMOD, #20H ; timer1 as 8-bit auto reload mode
    MOV AUXR, #40H ; timer1 work at 1T mode
    MOV TL1, #0FBH ; 115200 bps(256 - 18432000 / 32 / 115200)
    MOV TH1, #0FBH
    SETB TR1
    RET

;/////////////////////////////////////////////////////////////////////////////////////

INIT_SPI:
    MOV SPDAT, #0 ; initial SPI data
    MOV SPSTAT, #SPIF | WCOL ; clear SPI status
#ifdef MASTER
    MOV SPCTL, #SPEN | MSTR ; master mode
#else
    MOV SPCTL, #SPEN ; slave mode
#endif
RET

;/////////////////////////////////////////////////////////////////////////////////////

SEND_UART:
    JNB TI, $ ; wait pre-data sent
    CLR TI ; clear TI flag
    MOV SBUF, A ; send current data
    RET

;/////////////////////////////////////////////////////////////////////////////////////
RECV_UART:
    JNB    RI, $          ;wait receive complete
    CLR    RI            ;clear RI flag
    MOV    A, SBUF       ;return receive data
    RET
    RET

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

SPI_SWAP:
    #ifdef MASTER
    CLR    SPISS         ;pull low slave SS
    #endif
    MOV    SPDAT,A       ;trigger SPI send
    WAIT:
    MOV    A, SPSTAT     ;wait send complete
    JNB    ACC.7, WAIT    ;wait send complete
    MOV    SPSTAT, #SPIF | WCOL  ;clear SPI status
    #ifdef MASTER
    SETB   SPISS         ;push high slave SS
    #endif
    MOV    A, SPDAT      ;return received SPI data
    RET

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

END
11.5 SPI Function Demo (Single Master Single Slave) (C)

The following program, written in C language, tests SPI function and applies to SPI single master single slave configuration.

```c
#include "reg51.h"

#define MASTER              //define:master undefine:slave
#define FOSC 18432000L
#define BAUD (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int   WORD;
typedef unsigned long  DWORD;

sfr AUXR = 0x8e;          //Auxiliary register
sfr SPSTAT = 0xcd;         //SPI status register
#define SPIF 0x80              //SPSTAT.7
#define WCOL 0x40              //SPSTAT.6
sfr SPCTL = 0xce;          //SPI control register
#define SSIG 0x80               //SPCTL.7
#define SPEN 0x40               //SPCTL.6
#define DORD 0x20               //SPCTL.5
#define MSTR 0x10               //SPCTL.4
#define CPOL 0x08                //SPCTL.3
#define CPHA 0x04                //SPCTL.2
#define SPDHH 0x00            //CPU_CLK/4
#define SPDH 0x01               //CPU_CLK/16
#define SPDL 0x02               //CPU_CLK/64
#define SPDLL 0x03              //CPU_CLK/128
sfr SPDAT = 0xcf;          //SPI data register
sbit SPISS = P1^3;         //SPI slave select, connect to slave' SS(P1.4) pin
```
void InitUart();
void InitSPI();
void SendUart(BYTE dat); //send data to PC
BYTE RecvUart(); //receive data from PC
BYTE SPISwap(BYTE dat); //swap SPI data between master and slave

void main()
{
    InitUart(); //initial UART
    InitSPI(); //initial SPI

    while (1)
    {
        #ifdef MASTER //for master (receive UART data from PC and send it to slave,
        //in the meantime receive SPI data from slave and send it to PC)
            SendUart(SPISwap(RecvUart()));
        #else //for salve (receive SPI data from master and
        ACC = SPISwap(ACC); //send previous SPI data to master)
        #endif
    }
}

void InitUart()
{
    SCON = 0x5a; //set UART mode as 8-bit variable baudrate
    TMOD = 0x20; //timer1 as 8-bit auto reload mode
    AUXR = 0x40; //timer1 work at 1T mode
    TH1 = TL1 = BAUD; //115200 bps
    TR1 = 1;
}

void InitSPI()
{
    SPDAT = 0; //initial SPI data
    SPSTAT = SPIF | WCOL; //clear SPI status
    #ifdef MASTER //master mode
        SPCTL = SPEN | MSTR;
    #else //slave mode
        SPCTL = SPEN;
    #endif
}
void SendUart(BYTE dat)
{
    while (!TI);                  //wait pre-data sent
    TI = 0;                       //clear TI flag
    SBUF = dat;                   //send current data
}

BYTE RecvUart()
{
    while (!RI);                  //wait receive complete
    RI = 0;                       //clear RI flag
    return SBUF;                  //return receive data
}

BYTE SPISwap(BYTE dat)
{
    #ifdef MASTER
        SPISS = 0;                    //pull low slave SS
    #endif
    SPDAT = dat;                  //trigger SPI send
    while (!(SPSTAT & SPIF));     //wait send complete
    SPSTAT = SPIF | WCOL;        //clear SPI status
    #ifdef MASTER
        SPISS = 1;                    //push high slave SS
    #endif
    return SPDAT;                 //return received SPI data
}
11.6 SPI Demo (Single Master Multiple Slave) (ASM)

1. The demo program is suitable for single master multiple slave system
2. Hardware connection:

3. SPI communication:
8-bit Master MCU SPI register and 8-bit Slave MCU SPI register combined into a 16-bit cyclic shift register. When Master MCU is written a byte data to SPI data register (SPDAT), the data transmission is triggered immediately. With the SCLK’s clock signal, 8-bit data in Master MCU’s SPDAT register shift into Slave MCU’s SPDAT through MOSI pin, in the meanwhile, the 8-bit data in Slave MCU’s SPDAT register is shifted into Master MCU’s SPDAT register through MISO pin.
4. Modification method:
   a) Set “MASTER_SLAVE EQU 0”, then the object file is Master MCU file.
   b) Set “MASTER_SLAVE EQU 1”, then the object file is Slave #1 MCU file.
   c) Set “MASTER_SLAVE EQU 2”, then the object file is Slave #2 MCU file.
   d) Power-on the whole system (Master MCU, Slave #1 MCU and Slave #2 MCU)
   e) P1.2 and P1.3 respectively control Slave #1 and Slave #2, but still a moment, only one Slave MCU is selected.
   f) Using serial debugging assistant debug.
5. Using inquiry method to receive SPI data
6. Work environment: Fosc=18.432MHz and 9600 baudrate
;Define const
MASTER_SLAVE EQU 0 ;Master MCU
MASTER_SLAVE EQU 1 ;Slave #1 MCU
MASTER_SLAVE EQU 2 ;Slave #2 MCU

;RELOAD_8BIT_DATA EQU 0FFH ;56700@22.1184MHz
RELOAD_8BIT_DATA EQU 0FBH ;9600@18.432MHz
RELOAD_8BIT_DATA EQU 0F6H ;4800@18.432MHz
RELOAD_8BIT_DATA EQU 0FFH ;28800@11.0592MHz

;Define SFR
AUXR EQU 8EH ; Auxiliary register
SPCTL EQU 85H ;SPI control register
SPSTAT EQU 84H ;SPI status register
SPDAT EQU 86H ;SPI data register
EADC_SPI EQU IE.5 ;SPI interrupt enable bit

;Define SPI function pin
SCLK EQU P1.7 ;SPI clock pin
MISO EQU P1.6 ;SPI master input/slave output pin
MOSI EQU P1.5 ;SPI master output/slave input pin
SS EQU P1.4 ;SPI slave select pin
Slave1_SS EQU P1.2 ;slave #1 MCU select pin
Slave2_SS EQU P1.3 ;slave #2 MCU select pin
LED_MCU_START EQU P3.4 ;MCU work LED

;Define user variable
Flags EQU 20H ;user flag
SPI_Receive EQU Flags.0 ;SPI receive flag
T0_10mS_count EQU 30H ;10ms counter
SPI_buffer EQU 31H ;SPI receive buffer

;----------------------------------------------------------------
ORG 0000H
LJMP MAIN
ORG 000BH
LJMP timer0_Routine ;timer0 interrupt routine
ORG 002BH
LJMP ADC_SPI_Interrupt_Routine ;SPI interrupt routine
;----------------------------------------------------------------
ORG 0080H
MAIN:
CLR LED_MCU_START ;work led on
MOV SP,#7FH ;initial SP
ACALL Initial_System ;system initial
if MASTER_SLAVE == 0
CLR Slave1_SS ;select slave #1 MCU
Check_RS232:
    JNB    RI,Master_Check_SPI ;check UART receive
    ACALL  Get_Byte_From_RS232 ;load UART data to ACC
;    ACALL  RS232_Send_Byte ;send data in ACC to PC
;    SJMP  Check_RS232
    ACALL  SPI_Send_Byte ;send data in ACC to SPI slave
    SJMP  Check_RS232

Master_Check_SPI:
    JNB    SPI_Receive,Check_RS232 ;check SPI receive
    MOV    A,SPI_buffer ;load SPI data to ACC
    CLR    SPI_Receive ;clear SPI receive flag
    ACALL  SPI_Send_Byte ; send data in ACC to SPI slave
    SJMP  Check_RS232

else
Slave_Check_SPI:
    JNB    SPI_Receive,Slave_Check_SPI ;check SPI receive
    MOV    A,SPI_buffer ;load SPI data to ACC
    CLR    SPI_Receive ;clear SPI receive flag
    if MASTER_SLAVE == 2
    ADD    A,#1 ;value +1 on slave #2 MCU
    endif
    MOV    SPDAT,A;save data into SPDAT
    SJMP  Slave_Check_SPI

endif

if MASTER_SLAVE == 0
   timer0_Routine:
    PUSH  PSW
    PUSH  ACC
    MOV    TH0,#0C4H ;reload timer0 10ms value
    INC    T0_10mS_count ;10ms counter
    MOV    A,#200 ;count 200 times
    CLR    C
    SUBB   A,T0_10mS_count
    JNC    timer0_Exit
    CPL    SLAVE1_SS ;switch slave
    CPL    SLAVE2_SS
    MOV    T0_10mS_count,#0;reset counter
   timer0_Exit:
    POP    ACC
    POP    PSW
    RETI

else
   timer0_Routine:
    RETI
endif

;----------------------------------------------------------------
ADC_SPI_Interrupt_Routine:
  MOV  SPDAT,#0C0H ;clear SPIF and WCOL flag
  MOV  A,SPDAT  ;save SPI received data
  MOV  SPI_buffer,A
  SETB SPI_Receive ;set SPI receive flag
  RET

;------------------------------------------------------------------
Initial_System:
  ACALL  Initial_Uart  ;initial UART sfr
  ACALL  Initial_SPI  ;initial SPI sfr
  SETB TR0            ;start timer0
  SETB ET0            ;enable timer0 interrupt
  MOV  Flags,#0       ;initial flag
  SETB EA             ;enable global interrupt flag
  RET

;------------------------------------------------------------------
Initial_Uart:
  MOV  SCON,#50H       ;set UART as 8-bit variable mode
  MOV  TMOD,#21H       ;set timer mode
  MOV  TH1,#RELOAD_8BIT_DATA ;set UART baudrate
  MOV  TL1,#RELOAD_8BIT_DATA
  MOV  PCON,#80H       ;baudrate * 2
  ORL  AUXR,#40H        ;1T mode
  SETB TR1             ;timer1 start
  RET

;------------------------------------------------------------------
Initial_SPI:
  if MASTER_SLAVE == 0
    MOV  SPCTL,#11111100B ;master mode
  else
    MOV  SPCTL,#01101100B ;slave mode
  endif
  MOV  SPSTAT,#11000000B ;clear SPI flag
  ORL  AUXR,#08H        ;AUXR.3(ESPI) = 1
  SETB EADC_SPI        ;enable SPI interrupt
  RET

;------------------------------------------------------------------
RS232_Send_Byte:
  CLR  TI            ;ready send
  MOV  SBUF,A        ;write data to TX buffer
  JNB  TI,$          ;wait send completed
  CLR  TI            ;clear TI flag
  RET

;------------------------------------------------------------------
SPI_Send_Byte:
  CLR  EADC_SPI      ;disable SPI interrupt
  MOV  SPDAT,A       ;write data to SPI data register
SPI_Send_byte_Wait:
    MOV A,SPSTAT ;check SPI status
    ANL A,#80H
    JZ SPI_Send_byte_Wait ;wait SPI send complete
    SETB EADC_SPI ;enable SPI interrupt
    RET

Get_byte_From_RS232:
    MOV A,SBUF ;load data to ACC
    CLR RI ;clear UART receive flag
    RET

END

11.7 SPI Demo (Single Master Multiple Slave) (C)

/*-----------------------------------------------------------*/
/* --- STC MCU International Limited ------------------------*/
/* --- STC 1T Series MCU SPI ASM Demo ----------------------*/
/* --- Mobile: (86)13922805190 ------------------------------*/
/* --- Fax: 86-755-82944243 ----------------------------------*/
/* --- Tel: 86-755-82948412 -------------------------------*/
/* --- Web: www.STCMCU.com --------------------------------* /
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*-----------------------------------------------------------*/

typedef unsigned char INT8U;
typedef unsigned int INT16U;
typedef unsigned long INT32U;

#include "new_8051.h"

//Define const
#define SPI_INTERRUPT_VECTOR 9
#define TRUE 1
#define FALSE 0
#define MASTER
#define CONFIG_MASTER 0xd0 //master mode
#define CONFIG_SLAVE 0xc0 //slave mode
#define SPIF_WCOL_MASK 0xc0 //SPIF & WCOL mask bit
#define FOSC 1843200
#define BAUD 9600
#define BUF_SIZE 0x20
//Define SFR
sfr SPCTL = 0xce;

sbit LED_MCU_START = P3^4;  //work LED

bit SPI_Receive;  //SPI received flag

bit SPI_status;   //SPI status

INT8U SPI_buffer;         //SPI receive data buffer

INT8U RS232_point;

INT8U ISP_point;

INT8U buffer[BUF_SIZE];

//--------------------------------------------------------------------------------

void Initial_SPI();

void Init_System();

INT8U Get_Byte_From_RS232();

void RS232_Send_Byte(INT8U ch);

void SPI_Send_Byte(INT8U);

void send_buffer_to_PC();

void clear_buffer();

void delay(INT16U d);

void SPI_read_from_slave(INT8U n);

//--------------------------------------------------------------------------------

void main()
{

INT32U i=0;

LED_MCU_START = 0;     //work LED on

Init_System();        //system initial

SPI_Receive = 0;       //initial user flag

RS232_point = 0;

ISP_point = 0;

clear_buffer();        //empty buffer

#ifdef MASTER

while (1)
{

   if (RI)     //check UART RI
   {

      RI = 0;

      if (RS232_point < BUF_SIZE)
      {

         buffer[RS232_point++] = SBUF       //save UART RX data

      }

   }  

   if (i > 0)
   {

      i--;        //check wait

      if (i == 0)       //send all data at wait end
      {

         if (RS232_point > 0)
         {

            ISP_point = 0;

         }

      }

   }

#endif
SPI_status = 1; //1:SPI send
SPDAT = buffer[ISP_point++]; //trigger SPI send action
while (ISP_point < RS232_point); //other send in interrupt
}
delay(300);
SPI_read_from_slave(RS232_point); //read slave data
send_buffer_to_PC(); //send back to PC
clear_buffer();
SPI_Receive = 0;
RS232_point = 0;
ISP_point = 0;
RI = 0;
}
#endif
SPI_Receive = 0;
SPI_status = 0;    //0:SPI receive
RS232_point = 0;
ISP_point = 0;
while (1)
{
    if (SPI_Receive)
    {
        SPI_Receive = 0;
        i = 10000;   //wait another data
    }
    if (i > 0)
    {
        i--;
        if (i == 0)
        {
            if (!SPI_status) //SPI receive
            {
                RS232_point = ISP_point;
                ISP_point = 0;
                send_buffer_to_PC(); //send buffer data to PC
            }
            ISP_point = 0;
            SPI_status = 1; //1:SPI send
            SPI_Receive = 0;
            while (!SPI_Receive); //wait send the 1st data
delay(50);           //set timeout
clear_buffer();
RS232_point = 0;
ISP_point = 0;
SPI_status = 0;    //0:SPI receive
SPI_Receive = 0;
void SPI_Interrupt_Routine() interrupt SPI_INTERRUPT_VECTOR
{
    SPI_buffer = SPDAT;  //save SPI data
    SPSTAT = SPIF_WCOL_MASK;  //clear SPI flag
    SPI_Receive = 1;  //set SPI received flag
    if (SPI_status)  //1:SPI send
    {
        if (ISP_point < RS232_point)
        {
            SPDAT = buffer[ISP_point];
            ISP_point++;
        }
    }
    else  //0:SPI receive
    {
        if (ISP_point < BUF_SIZE)
        {
            buffer[ISP_point] = SPI_buffer;
            ISP_point++;
        }
    }
}

void Initial_RS232()
{
    ES = 0;
    SCON = 0x50;  //UART mode(8-bit variable)
    TMOD &= 0x0f;  //timer0 mode(8-bit auto-reload)
    TH1 = TL1 = 256 – FOSC/384/BAUD;  //UART baudrate
    TR1 = 1
    AUXR |= 0x40;  //1T mode
}

void Initial_SPI()
{
    #ifdef MASTER
        SPCTL = CONFIG_MASTER;  //master mode
    #else
        SPCTL = CONFIG_SLAVE;  //slave mode
    #endif
    SPSTAT = SPIF_WCOL_MASK;  //clear SPI flag
    IE2 |= 0x02;  //enable SPI interrupt
/***********************************************************************
void Init_System()
{
    Initial_RS232();    //initial UART
    Initial_SPI();    //initial SPI
    EA = 1;
}

/*************************************************************************
void RS232_Send_Byte(INT8U ch)
{
    TI = 0;     //ready send
    SBUF = ch;     //write UART data
    while (TI = 0);    //wait data sent
    TI = 0;     //clear TX flag
}

/*************************************************************************/
void send_buffer_to_PC()   //send all data in buffer to PC
{
    INT8U i;
    if (RS232_point == 0) return;
    RS232_Send_Byte(RS232_point);
    if (i=0; i<RS232_point; i++)
    {
        RS232_Send_Byte(buffer[i]);
    }
}

/*************************************************************************/
void clear_buffer()     //empty data buffer
{
    INT8U i;
    for (i=0; i<BUF_SIZE; i++)
    {
        buffer[i]  0
    }
}

/***************************************************************************/
void delay(INT16U d)
{
    INT16U i;
    while (d--)
    {
        i = 1000;
        while (i--);
    }
}
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Tel:086-755-82948412

Fax:86-755-82944243

//---------------------------------------------------------------#ifdef MASRER
void SPI_read_from_slave(INT8U n)		
//receive slave data
{
INT8U j;
clear_buffer()
SPI_status = 0;				
ISP_point = 0;
SPI_Receive = 0;
SPDAT = 0x00;				
while (!SPI_Receive);
SPI_Recevie = 0;
ISP_point = 0;				
for (j=0; j<n; j++)
{
		
SPDAT = 0x00;			
		
while (!SPI_Receive);
		
SPI_Receive = 0;
}
}
#endif

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STC MCU Limited.

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//0:SPI receive
//trigger SPI clock

d
e
t
i
im

//discard the 1st data

L

//trigger SPI clock

website：www.STCMCU.com


11.8 SPI Demo (Each other as the master-slave) (ASM)

;*-----------------------------------------------* /
;* --- STC MCU International Limited ----------------* /
;* --- STC 1T Series MCU SPI Demo(Each other as the master-slave) ---* /
;* --- Mobile: (86)13922805190 ----------------* /
;* --- Fax: 86-755-82944243 ----------------* /
;* --- Tel: 86-755-82948412 ----------------* /
;* --- Web: www.STCMCU.com ----------------* /
;* If you want to use the program or the program referenced in the artice, please specify in which data and procedures from STC ----* /
;*-----------------------------------------------* /

AUXR     DATA     08EH              ;Auxiliary register
SPSTAT   DATA     0CDH              ;SPI status register
SPIF     EQU      080H              ;SPSTAT.7
WCOL    EQU      040H              ;SPSTAT.6
SPCTL    DATA     0CEH              ;SPI control register
SSIG     EQU      080H              ;SPCTL.7
SPEN     EQU      040H              ;SPCTL.6
DORD     EQU      020H              ;SPCTL.5
MSTR     EQU      010H              ;SPCTL.4
CPOL     EQU      008H              ;SPCTL.3
CPHA     EQU      004H              ;SPCTL.2
SPDHH    EQU      000H              ;CPU_CLK/4
SPDH     EQU      001H              ;CPU_CLK/16
SPDL     EQU      002H              ;CPU_CLK/64
SPDLL    EQU      003H              ;CPU_CLK/128
SPDAT    DATA     0CFH              ;SPI data register
SPISS    BIT    P1.3              ;SPI slave select,connect to other MCU's SS(P1.4) pin

;////////////////////////////////////////////////////////////////////////////////////////////////////////////////////

ORG      0000H
LJMP     RESET
ORG      0100H
RESET:
LCALL    INIT_UART    ;initial UART
LCALL    INIT_SPI    ;initial SPI
MAIN:
JB       RI, MASTER_MODE
SLAVE_MODE:
MOV      A, SPSTAT
JNB      ACC.7, MAIN
MOV      SPSTAT, #SPIF | WCOL    ;clear SPI status
MOV      SPDAT, SPDAT    ;return received SPI data
SJMP     MAIN
MASTER_MODE:

MOVE SPCTL, #SPEN | MSTR ;set as master
LCALL RECV_UART ;receive UART data from PC
LCALL SPI_SWAP ;send it to slave, in the meantime, receive SPI data from slave
LCALL SEND_UART ;send SPI data to PC
MOVE SPCTL, #SPEN ;reset as slave
SJMP MAIN

;//////////////////////////////////////////////////////////////////////////////////////////
INIT_UART:

MOVE SCON, #5AH ;set UART mode as 8-bit variable baudrate
MOVE TMOD, #20H ;timer1 as 8-bit auto reload mode
MOVE AUXR, #40H ;timer1 work at 1T mode
MOVE TL1, #0FBH ;115200 bps(256 - 18432000 / 32 / 115200)
MOVE TH1, #0FBH
SETB TR1
RET

;//////////////////////////////////////////////////////////////////////////////////////////
INIT_SPI:

MOVE SPDAT, #0 ;initial SPI data
MOVE SPSTAT, #SPIF | WCOL ;clear SPI status
MOVE SPCTL, #SPEN ;slave mode
RET

;//////////////////////////////////////////////////////////////////////////////////////////
SEND_UART:

JNB TI, $ ;wait pre-data sent
CLR TI ;clear TI flag
MOVE SBUF, A ;send current data
RET

;//////////////////////////////////////////////////////////////////////////////////////////
RECV_UART:

JNB RI, $ ;wait receive complete
CLR RI ;clear RI flag
MOVE A, SBUF ;return receive data
RET

;//////////////////////////////////////////////////////////////////////////////////////////
SPI_SWAP:

CLR SPISS ;pull low slave SS
MOVE SPDAT, A ;trigger SPI send

WAIT:

MOVE A, SPSTAT
JNB ACC.7, WAIT ;wait send complete
MOVE SPSTAT, #SPIF | WCOL ;clear SPI status
SETB SPISS ;push high slave SS
MOVE A, SPDAT ;return received SPI data
RET

;//////////////////////////////////////////////////////////////////////////////////////////
END
11.9 SPI Demo (Each other as the master-slave) (C)

/*-----------------------------------------------*/
/* --- STC MCU International Limited */
/* --- STC 1T Series MCU SPI Demo(Each other as the master-slave) */
/* --- Mobile: (86)13922805190 */
/* --- Fax: 86-755-82944243 */
/* --- Tel: 86-755-82948412 */
/* --- Web: www.STCMCU.com */
/* If you want to use the program or the program referenced in the article, please specify in which data and procedures from STC */

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

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#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

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typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
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#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

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typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
#define WCOL  0x40          //SPSTAT.6
sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"

#include "reg51.h"

#define FOSC  18432000L
#define BAUD  (256 - FOSC / 32 / 115200)

typedef unsigned char  BYTE;
typedef unsigned int    WORD;
typedef unsigned long  DWORD;

sfr AUXR  =   0x8e;         //Auxiliary register
sfr SPSTAT =   0xcd;         //SPI status register
#define SPIF  0x80          //SPSTAT.7
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sfr S PCTL  =   0xce;         //SPI control register
#define SSIG     0x80          //SPCTL.7
#define SPEN   0x40           //SPCTL.6
#define DORD   0x20          //SPCTL.5
#define MSTR   0x10          //SPCTL.4
#define CPOL  0x08          //SPCTL.3
#define CPHA   0x04          //SPCTL.2
#define SPDHH   0x00          //CPU_CLK/4
#define SPDH   0x01          //CPU_CLK/16
#define SPDL   0x02          //CPU_CLK/64
#define SPDLL  0x03          //CPU_CLK/128
sfr SPDAT  =   0xcf;         //SPI data register
sbit SPISS   =   P1^3;         //SPI slave select, connect to other MCU's SS(P1.4) pin

#include "reg51.h"
void main()
{
    InitUart();               //initial UART
    InitSPI();                //initial SPI

    while (1)
    {
        if (RI)
        {
            SPCTL = SPEN | MSTR;  //set as master
            SendUart(SPISwap(RecvUart()));
            SPCTL = SPEN;         //reset as slave
        }
        if (SPSTAT & SPIF)
        {
            SPSTAT = SPIF | WCOL;  //clear SPI status
            SPDAT = SPDAT;         //move data from receive buffer to send buffer
            SPCTL = SPEN;          //reset as slave
        }
    }
}

void InitUart()
{
    SCON = 0x5a;                //set UART mode as 8-bit variable baudrate
    TMOD = 0x20;                //timer1 as 8-bit auto reload mode
    AUXR = 0x40;                //timer1 work at 1T mode
    TH1 = TL1 = BAUD;           //115200 bps
    TR1 = 1;
}

void InitSPI()
{
    SPDAT = 0;                  //initial SPI data
    SPSTAT = SPIF | WCOL;       //clear SPI status
    SPCTL = SPEN;               //slave mode
}
void SendUart(BYTE dat)
{
    while (!TI); //wait pre-data sent
    TI = 0;     //clear TI flag
    SBUF = dat; //send current data
}

BYTE RecvUart()
{
    while (!RI); //wait receive complete
    RI = 0;     //clear RI flag
    return SBUF; //return receive data
}

BYTE SPISwap(BYTE dat)
{
    SPISS = 0; //pull low slave SS
    SPDAT = dat; //trigger SPI send
    while (!((SPSTAT & SPIF))); //wait send complete
    SPSTAT = SPIF | WCOL; //clear SPI status
    SPISS = 1; //push high slave SS
    return SPDAT; //return received SPI data
}
Chapter 12 IAP / EEPROM

The ISP in STC12C5Axx series makes it possible to update the user’s application program and non-volatile application data (in IAP-memory) without removing the MCU chip from the actual end product. This useful capability makes a wide range of field-update applications possible. (Note ISP needs the loader program pre-programmed in the ISP-memory.) In general, the user needn’t know how ISP operates because STC has provided the standard ISP tool and embedded ISP code in STC shipped samples. But, to develop a good program for ISP function, the user has to understand the architecture of the embedded flash.

The embedded flash consists of 16 pages. Each page contains 512 bytes. Dealing with flash, the user must erase it in page unit before writing (programming) data into it. Erasing flash means setting the content of that flash as FFh. Two erase modes are available in this chip. One is mass mode and the other is page mode. The mass mode gets more performance, but it erases the entire flash. The page mode is something performance less, but it is flexible since it erases flash in page unit. Unlike RAM’s real-time operation, to erase flash or to write (program) flash often takes long time so to wait finish.

Furthermore, it is a quite complex timing procedure to erase/program flash. Fortunately, the STC12C5A60S2 series carried with convenient mechanism to help the user read/change the flash content. Just filling the target address and data into several SFR, and triggering the built-in ISP automation, the user can easily erase, read, and program the embedded flash.

The In-Application Program feature is designed for user to Read/Write nonvolatile data flash. It may bring great help to store parameters those should be independent of power-up and power-done action. In other words, the user can store data in data flash memory, and after he shutting down the MCU and rebooting the MCU, he can get the original value, which he had stored in.

The user can program the data flash according to the same way as ISP program, so he should get deeper understanding related to SFR IAP_DATA, IAP_ADDRH, IAP_ADDRL, IAP_CMD, IAP_TRIG, and IAP_CONTR.

12.1 IAP / ISP Control Register

The following special function registers are related to the IAP/ISP operation. All these registers can be accessed by software in the user’s application program.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Address</th>
<th>Bit Address and Symbol</th>
<th>Value after Power-on or Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>IAP_DATA</td>
<td>ISP/IAP Flash Data Register</td>
<td>C2H</td>
<td>MSB 1111 1111B</td>
<td></td>
</tr>
<tr>
<td>IAP_ADDRH</td>
<td>ISP/IAP Flash Address High</td>
<td>C3H</td>
<td>MSB 0000 0000B</td>
<td></td>
</tr>
<tr>
<td>IAP_ADDRL</td>
<td>ISP/IAP Flash Address Low</td>
<td>C4H</td>
<td>MSB 0000 0000B</td>
<td></td>
</tr>
<tr>
<td>IAP_CMD</td>
<td>ISP/IAP Flash Command Register</td>
<td>C5H</td>
<td>MSB xxxx x000B</td>
<td></td>
</tr>
<tr>
<td>IAP_TRIG</td>
<td>ISP/IAP Flash Command Trigger</td>
<td>C6H</td>
<td>MSB xxxxx xxxxB</td>
<td></td>
</tr>
<tr>
<td>IAP_CONTR</td>
<td>ISP/IAP Control Register</td>
<td>C7H</td>
<td>MSB 0000 x000B</td>
<td></td>
</tr>
<tr>
<td>PCON</td>
<td>Power Control</td>
<td>87H</td>
<td>MSB 0011 0000B</td>
<td></td>
</tr>
</tbody>
</table>
IAP_DATA: ISP/IAP Flash Data Register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IAP_DATA is the data port register for ISP/IAP operation. The data in IAP_DATA will be written into the desired address in operating ISP/IAP write and it is the data window of readout in operating ISP/IAP read.

IAP_ADDRH: ISP/IAP Flash Address High

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IAP_ADDRH is the high-byte address port for all ISP/IAP modes. IAP_ADDRH[7:5] must be cleared to 000, if one bit of IAP_ADDRH[7:5] is set, the ISP/ISP write function must fail.

IAP_ADDRL: ISP/IAP Flash Address Low

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IAP_ADDRL is the low port for all ISP/IAP modes. In page erase operation, it is ignored.

IAP_CMD: ISP/IAP Flash-operating Mode Command Register

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>MS1</td>
</tr>
</tbody>
</table>

B7–B2: Reserved.
MS1, MS0 : ISP/IAP operating mode selection. IAP_CMD is used to select the flash mode for performing numerous ISP/IAP function or used to access protected SFRs.

0, 0 : Standby
0, 1 : Data Flash/EEPROM read.
1, 0 : Data Flash/EEPROM program.
1, 1 : Data Flash/EEPROM page erase.

IAP_TRIG: ISP/IAP Flash Command Trigger Register.

<table>
<thead>
<tr>
<th>bit</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IAP_TRIG is the command port for triggering ISP/IAP activity and protected SFRs access. If IAP_TRIG is filled with sequential 0x5Ah, 0xA5h and if IAPEN(IAP_CONTR.7) = 1, ISP/IAP activity or protected SFRs access will triggered.
IAP_CONTR: ISP/IAP Control Register

<table>
<thead>
<tr>
<th>bit</th>
<th>name</th>
<th>B7</th>
<th>B6</th>
<th>B5</th>
<th>B4</th>
<th>B3</th>
<th>B2</th>
<th>B1</th>
<th>B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>name</td>
<td>IAPEN</td>
<td>SWBS</td>
<td>SWRST</td>
<td>CMD_FAIL</td>
<td>-</td>
<td>WT2</td>
<td>WT1</td>
<td>WT0</td>
<td></td>
</tr>
</tbody>
</table>

IAPEN: ISP/IAP operation enable.
0: Global disable all ISP/IAP program/erase/read function.
1: Enable ISP/IAP program/erase/read function.

SWBS: software boot selection control.
0: Boot from main-memory after reset.
1: Boot from ISP memory after reset.

SWRST: software reset trigger control.
0: No operation
1: Generate software system reset. It will be cleared by hardware automatically.

CMD_FAIL: Command Fail indication for ISP/IAP operation.
0: The last ISP/IAP command has finished successfully.
1: The last ISP/IAP command fails. It could be caused since the access of flash memory was inhibited.

B3: Reserved. Software must write “0” on this bit when IAP_CONTR is written.

WT2~WT0: Waiting time selection while flash is busy.

<table>
<thead>
<tr>
<th>Setting wait times</th>
<th>CPU wait times</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>Program &lt;= 55μS</td>
</tr>
<tr>
<td>WT2</td>
<td>WT1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: Software reset actions could reset other SFR, but it never influences bits IAPEN and SWBS. The IAPEN and SWBS only will be reset by power-up action, while not software reset.

12.2 Using EX_LVD to detect whether data need to be saved

If power inputting source is 220V AC, then the reference application circuit as bellow:

![Circuit Diagram]

Note: 7805 output 8.5V voltage and use R1 and R2 can achieve the low voltage detect function at low threshold voltage. Program can use query mode or interrupt mode to check LVDF flag. The detailed implementation is clear LVDF at first and then read LVDF again, if LVDF is still 1, then maybe low voltage, you should save data immediately. After saved completed, check LVDF continue. If LVDF is 1 then wait for voltage restoration, else if LVDF is 0, then you can go other function code.
### 12.3 STC12C5A60S2 series internal EEPROM allocation table

<table>
<thead>
<tr>
<th>Type</th>
<th>EEPROM (Byte)</th>
<th>Sector Numbers</th>
<th>Begin_Sector Begin_Address</th>
<th>End_Sector End_Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>STC12C5A08S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12C5A16S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12C5A20S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12C5A32S2/AD/PWM</td>
<td>28K</td>
<td>56</td>
<td>0000H</td>
<td>6FFFH</td>
</tr>
<tr>
<td>STC12C5A40S2/AD/PWM</td>
<td>20K</td>
<td>40</td>
<td>0000H</td>
<td>4FFFH</td>
</tr>
<tr>
<td>STC12C5A48S2/AD/PWM</td>
<td>12K</td>
<td>24</td>
<td>0000H</td>
<td>2FFFH</td>
</tr>
<tr>
<td>STC12C5A52S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12C5A56S2/AD/PWM</td>
<td>4K</td>
<td>8</td>
<td>0000H</td>
<td>0FFFH</td>
</tr>
<tr>
<td>STC12C5A60S2/AD/PWM</td>
<td>1K</td>
<td>2</td>
<td>0000H</td>
<td>03FFFH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>EEPROM (Byte)</th>
<th>Sector Numbers</th>
<th>Begin_Sector Begin_Address</th>
<th>End_Sector End_Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>STC12LE5A08S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12LE5A16S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12LE5A20S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12LE5A32S2/AD/PWM</td>
<td>28K</td>
<td>56</td>
<td>0000H</td>
<td>6FFFH</td>
</tr>
<tr>
<td>STC12LE5A40S2/AD/PWM</td>
<td>20K</td>
<td>40</td>
<td>0000H</td>
<td>4FFFH</td>
</tr>
<tr>
<td>STC12LE5A48S2/AD/PWM</td>
<td>12K</td>
<td>24</td>
<td>0000H</td>
<td>2FFFH</td>
</tr>
<tr>
<td>STC12LE5A52S2/AD/PWM</td>
<td>8K</td>
<td>16</td>
<td>0000H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>STC12LE5A56S2/AD/PWM</td>
<td>4K</td>
<td>8</td>
<td>0000H</td>
<td>0FFFH</td>
</tr>
<tr>
<td>STC12LE5A60S2/AD/PWM</td>
<td>1K</td>
<td>2</td>
<td>0000H</td>
<td>03FFFH</td>
</tr>
</tbody>
</table>

### STC12C5A32S2/AD/PWM address reference table in detail (512 bytes per sector)

<table>
<thead>
<tr>
<th>Sector</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0000H</td>
<td>01FFH</td>
</tr>
<tr>
<td>2</td>
<td>0200H</td>
<td>03FFH</td>
</tr>
<tr>
<td>3</td>
<td>0400H</td>
<td>05FFH</td>
</tr>
<tr>
<td>4</td>
<td>0600H</td>
<td>07FFH</td>
</tr>
<tr>
<td>5</td>
<td>0800H</td>
<td>09FFH</td>
</tr>
<tr>
<td>6</td>
<td>0A00H</td>
<td>0BFFH</td>
</tr>
<tr>
<td>7</td>
<td>0C00H</td>
<td>0DFFH</td>
</tr>
<tr>
<td>8</td>
<td>0E00H</td>
<td>0FFFH</td>
</tr>
<tr>
<td>9</td>
<td>1000H</td>
<td>11FFH</td>
</tr>
<tr>
<td>10</td>
<td>1200H</td>
<td>13FFH</td>
</tr>
<tr>
<td>11</td>
<td>1400H</td>
<td>15FFH</td>
</tr>
<tr>
<td>12</td>
<td>1600H</td>
<td>17FFH</td>
</tr>
<tr>
<td>13</td>
<td>1800H</td>
<td>19FFH</td>
</tr>
<tr>
<td>14</td>
<td>1A00H</td>
<td>1BFFH</td>
</tr>
<tr>
<td>15</td>
<td>1C00H</td>
<td>1DFFH</td>
</tr>
<tr>
<td>16</td>
<td>1E00H</td>
<td>1FFFH</td>
</tr>
<tr>
<td>17</td>
<td>2000H</td>
<td>21FFH</td>
</tr>
<tr>
<td>18</td>
<td>2200H</td>
<td>23FFH</td>
</tr>
<tr>
<td>19</td>
<td>2400H</td>
<td>25FFH</td>
</tr>
<tr>
<td>20</td>
<td>2600H</td>
<td>27FFH</td>
</tr>
<tr>
<td>21</td>
<td>2800H</td>
<td>29FFH</td>
</tr>
<tr>
<td>22</td>
<td>2A00H</td>
<td>2BFFH</td>
</tr>
<tr>
<td>23</td>
<td>2C00H</td>
<td>2DFFH</td>
</tr>
<tr>
<td>24</td>
<td>2E00H</td>
<td>2FFFH</td>
</tr>
<tr>
<td>Sector 25</td>
<td>Sector 26</td>
<td>Sector 27</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>----------</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>3000H</td>
<td>31FFH</td>
<td>3200H</td>
</tr>
<tr>
<td>3400H</td>
<td>35FFH</td>
<td>3600H</td>
</tr>
<tr>
<td>Sector 29</td>
<td>Sector 30</td>
<td>Sector 31</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>3800H</td>
<td>39FFH</td>
<td>3A00H</td>
</tr>
<tr>
<td>3C00H</td>
<td>3DFFH</td>
<td>3E00H</td>
</tr>
<tr>
<td>Sector 33</td>
<td>Sector 34</td>
<td>Sector 35</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>4000H</td>
<td>41FFH</td>
<td>4200H</td>
</tr>
<tr>
<td>4400H</td>
<td>45FFH</td>
<td>4600H</td>
</tr>
<tr>
<td>Sector 37</td>
<td>Sector 38</td>
<td>Sector 39</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>4800H</td>
<td>49FFH</td>
<td>4A00H</td>
</tr>
<tr>
<td>4C00H</td>
<td>4DFFH</td>
<td>4E00H</td>
</tr>
<tr>
<td>Sector 41</td>
<td>Sector 42</td>
<td>Sector 43</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>5000H</td>
<td>51FFH</td>
<td>5200H</td>
</tr>
<tr>
<td>5400H</td>
<td>55FFH</td>
<td>5600H</td>
</tr>
<tr>
<td>Sector 45</td>
<td>Sector 46</td>
<td>Sector 47</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>5800H</td>
<td>59FFH</td>
<td>5A00H</td>
</tr>
<tr>
<td>5C00H</td>
<td>5DFFH</td>
<td>5E00H</td>
</tr>
<tr>
<td>Sector 49</td>
<td>Sector 50</td>
<td>Sector 51</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>6000H</td>
<td>61FFH</td>
<td>6200H</td>
</tr>
<tr>
<td>6400H</td>
<td>65FFH</td>
<td>6600H</td>
</tr>
<tr>
<td>Sector 53</td>
<td>Sector 54</td>
<td>Sector 55</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
</tr>
<tr>
<td>6800H</td>
<td>69FFH</td>
<td>6A00H</td>
</tr>
<tr>
<td>6C00H</td>
<td>6DFFH</td>
<td>6E00H</td>
</tr>
</tbody>
</table>
12.4 IAP/EEPROM Assembly Language Program Introduction

; /*It is decided by the assembler/compiler used by users that whether the SFRs addresses are declared by the
DATA or the EQU directive*/
IAP_DATA  DATA  0C2H or IAP_DATA  EQU  0C2H
IAP_ADDRH DATA  0C3H or IAP_ADDRH EQU 0C3H
IAP_ADDRL DATA  0C4H or IAP_ADDRL EQU 0C4H
IAP_CMD DATA  0C5H or IAP_CMD EQU 0C5H
IAP_TRIG DATA  0C6H or IAP_TRIG EQU 0C6H
IAP_CONTR DATA  0C7H or IAP_CONTR EQU 0C7H

; /*Define ISP/IAP/EEPROM command and wait time*/
ISP_IAP_BYTE_READ  EQU 1 ; Byte-Read
ISP_IAP_BYTE_PROGRAM EQU 2 ; Byte-Program
ISP_IAP_SECTOR_ERASE  EQU 3 ; Sector-Erase
WAIT_TIME   EQU 0 ; Set wait time

; /*Byte-Read*/
MOV  IAP_ADDRH, #BYTE_ADDR_HIGH ; Set ISP/IAP/EEPROM address high
MOV  IAP_ADDRL, #BYTE_ADDR_LOW ; Set ISP/IAP/EEPROM address low
MOV  IAP_CONTR, #WAIT_TIME ; Set wait time
ORL  IAP_CONTR, #10000000B ; Open ISP/IAP function
MOV  IAP_CMD, #ISP_IAP_BYTE_READ ; Set ISP/IAP Byte-Read command
MOV  IAP_TRIG, #5AH ; Send trigger command1 (0x5a)
MOV  IAP_TRIG, #0A5H ; Send trigger command2 (0xa5)
NOP ; CPU will hold here until ISP/IAP/EEPROM operation complete
MOV  A, IAP_DATA ; Read ISP/IAP/EEPROM data

; /*Disable ISP/IAP/EEPROM function, make MCU in a safe state*/
MOV  IAP_CONTR, #00000000B ; Close ISP/IAP/EEPROM function
MOV  IAP_CMD, #00000000B ; Clear ISP/IAP/EEPROM command
MOV  IAP_TRIG, #00000000B ; Clear trigger register to prevent mistrigger
MOV  IAP_ADDRH, #0FFH ; Move 00 into address high-byte unit,
MOV    IAP_ADDRL, #0FFH ; Data ptr point to non-EEPROM area,

; /*Byte-Program, if the byte is null(0FFH), it can be programmed; else, MCU must operate Sector-Erase firstly,
and then can operate Byte-Program.*/
MOV  IAP_DATA, #ONE_DATA ; Write ISP/IAP/EEPROM data
MOV  IAP_ADDRH, #BYTE_ADDR_HIGH ; Set ISP/IAP/EEPROM address high
MOV  IAP_ADDRL, #BYTE_ADDR_LOW ; Set ISP/IAP/EEPROM address low
MOV  IAP_CONTR, #WAIT_TIME ; Set wait time
ORL  IAP_CONTR, #10000000B ; Open ISP/IAP function
MOV  IAP_CMD, #ISP_IAP_BYTE_READ ; Set ISP/IAP Byte-Read command
MOV  IAP_TRIG, #5AH ; Send trigger command1 (0x5a)
MOV  IAP_TRIG, #0A5H ; Send trigger command2 (0xa5)
NOP ; CPU will hold here until ISP/IAP/EEPROM operation complete
; /*Disable ISP/IAP/EEPROM function, make MCU in a safe state*/
MOV  IAP_CONTR, #00000000B
MOV  IAP_CMD, #00000000B
;MOV  IAP_TRIG, #00000000B
;MOV  IAP_ADDRH, #FFH
;MOV  IAP_ADDRL, #0FFH

; /*Erase one sector area, there is only Sector-Erase instead of Byte-Erase, every sector area account for 512 bytes*/
MOV  IAP_ADDRH, #SECTOT_FIRST_BYTE_ADDR_HIGH  
MOV  IAP_ADDRL, #SECTOT_FIRST_BYTE_ADDR_LOW
MOV  IAP_CONTR, #WAIT_TIME
ORL  IAP_CONTR, #10000000B
MOV  IAP_CMD, #ISP_IAP_SECTOR_ERASE
MOV  IAP_TRIG, #5AH
MOV  IAP_TRIG, #0A5H
NOP

; /*Disable ISP/IAP/EEPROM function, make MCU in a safe state*/
MOV  IAP_CONTR, #00000000B
MOV  IAP_CMD, #00000000B
;MOV  IAP_TRIG, #00000000B
;MOV  IAP_ADDRH, #0FFH
;MOV  IAP_ADDRL, #0FFH
12.5EEPROMDemoProgramwritteninAssemblyLanguage

/**----------------------------------------------------------*/
/** --- STC MCU International Limited -------------------------*/
/** --- STC 1T Series MCU ISP/IAP/EEPROM Demo ----------------*/
/** --- Mobile: (86)13922805190 -------------------------------*/
/** --- Fax: 86-755-82944243 -------------------------------*/
/** --- Tel: 86-755-82948412 -------------------------------*/
/** --- Web: www.STCMCU.com --------------------------------*/
/** If you want to use the program or the program referenced in the */
/** article, please specify in which data and procedures from STC */
/**----------------------------------------------------------------*/

/**Declare SFRs associated with the IAP*/
IAP_DATA EQU 0C2H ;Flash data register
IAP_ADDRH EQU 0C3H ;Flash address HIGH
IAP_ADDRL EQU 0C4H ;Flash address LOW
IAP_CMD EQU 0C5H ;Flash command register
IAP_TRIG EQU 0C6H ;Flash command trigger
IAP_CONTR EQU 0C7H ;Flash control register

/**Define ISP/IAP/EEPROM command*/
CMD_IDLE EQU 0 ;Stand-By
CMD_READ EQU 1 ;Byte-Read
CMD_PROGRAM EQU 2 ;Byte-Program
CMD_ERASE EQU 3 ;Sector-Erase

/**Define ISP/IAP/EEPROM operation const for IAP_CONTR*/
;ENABLE_IAP EQU 80H ;if SYSCLK<30MHz
;ENABLE_IAP EQU 81H ;if SYSCLK<24MHz
ENABLE_IAP EQU 82H ;if SYSCLK<20MHz
;ENABLE_IAP EQU 83H ;if SYSCLK<12MHz
;ENABLE_IAP EQU 84H ;if SYSCLK<6MHz
;ENABLE_IAP EQU 85H ;if SYSCLK<3MHz
;ENABLE_IAP EQU 86H ;if SYSCLK<2MHz
;ENABLE_IAP EQU 87H ;if SYSCLK<1MHz

/**Start address for STC12C5A60S2 EEPROM*/
IAP_ADDRESS EQU 0000H

;------------------------------------------------------------
ORG 0000H
LJMP MAIN
;------------------------------------------------------------
ORG 0100H

MAIN:
MOV P1, #0FEH ;1111,1110 System Reset OK
LCALL DELAY ;Delay
;-------------------------------
MOV     DPTR, #IAP_ADDRESS          ;Set ISP/IAP/EEPROM address
LCALL    IAP_ERASE                  ;Erase current sector
;-------------------------------
MOV     DPTR, #IAP_ADDRESS          ;Set ISP/IAP/EEPROM address
MOV     R0, #0                       ;Set counter (512)
MOV     R1, #2
CHECK1:                                  ;Check whether all sector data is FF
LCALL   IAP_READ                  ;Read Flash
CJNE   A, #0FFH, ERROR              ;If error, break
INC    DPTR                        ;Inc Flash address
DJNZ    R0, CHECK1                  ;Check next
DJNZ    R1, CHECK1                  ;Check next
;-------------------------------
MOV     P1, #0FCH                    ;1111,1100 Erase successful
LCALL   DELAY                       ;Delay
;-------------------------------
MOV     DPTR, #IAP_ADDRESS          ;Set ISP/IAP/EEPROM address
MOV     R0, #0                       ;Set counter (512)
MOV     R1, #2
MOV     R2, #0                       ;Initial test data
NEXT:                                    ;Program 512 bytes data into data flash
MOV     A, R2                        ;Ready IAP data
LCALL   IAP_PROGRAM                 ;Program flash
INC     DPTR                        ;Inc Flash address
INC     R2                           ;Modify test data
DJNZ    R0, NEXT                     ;Program next
DJNZ    R1, NEXT                     ;Program next
;-------------------------------
MOV    P1, #0F8H                    ;1111,1000 Program successful
SJMP    $                           ;1111,0000 Verify successful
;-------------------------------
MOV     DPTR, #IAP_ADDRESS         ;Set ISP/IAP/EEPROM address
MOV     R0, #0                       ;Set counter (512)
MOV     R1, #2
MOV     R2, #0
CHECK2:                                  ;Verify 512 bytes data
LCALL   IAP_READ                    ;Read Flash
CJNE    A,    2,     ERROR                   ;If error, break
INC    DPTR                        ;Inc Flash address
INC    R2                           ;Modify verify data
DJNZ    R0, CHECK2                  ;Check next
DJNZ  R1, CHECK2                  ;Check next
;-------------------------------
MOV    P1, #0F0H                    ;1111,0000 Verify successful
;-------------------------------
ERROR:
  MOV  P0,  R0
  MOV  P2,  R1
  MOV  P3,  R2
  CLR     P1.7                        ;0xxx,xxx IAP operation fail
  SJMP   $

;/*------------------------
;Software delay function
;------------------------*/
DELAY:
  CLR     A
  MOV    R0,  A
  MOV    R1,  A
  MOV    R2,  #20H
DELAY1:
  DJNZ   R0,  DELAY1
  DJNZ  R1,  DELAY1
  DJNZ  R2,  DELAY1
  RET

;/*------------------------
;Disable ISP/IAP/EEPROM function
;Make MCU in a safe state
;------------------------*/
IAP_IDLE:
  MOV  IAP_CONTR,  #0              ;Close IAP function
  MOV  IAP_CMD,  #0              ;Clear command to standby
  MOV  IAP_TRIG,  #0     ;Clear trigger register
  MOV  IAP_ADDRH,  #80H      ;Data ptr point to non-EEPROM area
  MOV   IAP_ADDRL,  #0          ;Clear IAP address to prevent misuse
  RET

;/*------------------------
;Read one byte from ISP/IAP/EEPROM area
;Input: DPTR(ISP/IAP/EEPROM address)
;Output:ACC (Flash data)
;------------------------*/
IAP_READ:
  MOV  IAP_CONTR,  #ENABLE_IAP  ;Open IAP function, and set wait time
  MOV  IAP_CMD,  #CMD_READ        ;Set ISP/IAP/EEPROM READ command
  MOV  IAP_ADDRH,  #80H      ;Set ISP/IAP/EEPROM address low
  MOV   IAP_ADDRL,  #0          ;Set ISP/IAP/EEPROM address high
  MOV  IAP_TRIG,  #5AH              ;Send trigger command1 (0x5a)
  MOV  IAP_TRIG,  #0A5H            ;Send trigger command2 (0xa5)
  NOP                             ;MCU will hold here until ISP/IAP/EEPROM operation complete
  MOV    A,  IAP_DATA                 ;Read ISP/IAP/EEPROM data
  LCALL  IAP_IDLE                    ;Close ISP/IAP/EEPROM function
  RET
;/*----------------------------
;Program one byte to ISP/IAP/EEPROM area
;Input: DPAT(ISP/IAP/EEPROM address)
;ACC (ISP/IAP/EEPROM data)
;Output:-
;----------------------------*/
IAP_PROGRAM:
    MOV    IAP_CONTR, #ENABLE_IAP         ;Open IAP function, and set wait time
    MOV    IAP_CMD, #CMD_PROGRAM    ;Set ISP/IAP/EEPROM PROGRAM command
    MOV    IAP_ADDRL, DPL                  ;Set ISP/IAP/EEPROM address low
    MOV    IAP_ADDRH, DPH                  ;Set ISP/IAP/EEPROM address high
    MOV    IAP_DATA, A                    ;Write ISP/IAP/EEPROM data
    MOV    IAP_TRIG, #5AH             ;Send trigger command1 (0x5a)
    MOV    IAP_TRIG, #0A5H            ;Send trigger command2 (0xa5)
    NOP                          ;MCU will hold here until ISP/IAP/EEPROM operation complete
    LCALL  IAP_IDLE                   ;Close ISP/IAP/EEPROM function
    RET

;/*----------------------------
;Erase one sector area
;Input: DPTR(ISP/IAP/EEPROM address)
;Output:-
;----------------------------*/
IAP_ERASE:
    MOV    IAP_CONTR, #ENABLE_IAP     ;Open IAP function, and set wait time
    MOV    IAP_CMD, #CMD_ERASE      ;Set ISP/IAP/EEPROM ERASE command
    MOV    IAP_ADDRL, DPL             ;Set ISP/IAP/EEPROM address low
    MOV    IAP_ADDRH, DPH             ;Set ISP/IAP/EEPROM address high
    MOV    IAP_TRIG, #5AH             ;Send trigger command1 (0x5a)
    MOV    IAP_TRIG, #0A5H            ;Send trigger command2 (0xa5)
    NOP                            ;MCU will hold here until ISP/IAP/EEPROM operation complete
    LCALL  IAP_IDLE                   ;Close ISP/IAP/EEPROM function
    RET

END
12.6 EEPROM Demo Program written in C Language
/*------------------------------------------*/
/* --- STC MCU International Limited */
/* --- STC 1T Series MCU ISP/IAP/EEPROM Demo */
/* --- Mobile: (86)13922805190 */
/* --- Fax: 86-755-82944243 */
/* --- Tel: 86-755-82948412 */
/* --- Web: www.STCMCU.com */
/* If you want to use the program or the program referenced in the */
/* article, please specify in which data and procedures from STC */
/*------------------------------------------*/

#include "reg51.h"
#include "intrins.h"

typedef unsigned char BYTE;
typedef unsigned int WORD;

/*Declare SFR associated with the IAP*/
sfr IAP_DATA = 0xC2; //Flash data register
sfr IAP_ADDRH = 0xC3; //Flash address HIGH
sfr IAP_ADDRL = 0xC4; //Flash address LOW
sfr IAP_CMD = 0xC5; //Flash command register
sfr IAP_TRIG = 0xC6; //Flash command trigger
sfr IAP_CONTR = 0xC7; //Flash control register

/*Define ISP/IAP/EEPROM command*/
define CMD_IDLE 0 //Stand-By
define CMD_READ 1 //Byte-Read
define CMD_PROGRAM 2 //Byte-Program
#define CMD_ERASE 3 //Sector-Erase

/*Define ISP/IAP/EEPROM operation const for IAP_CONTR*/
//define ENABLE_IAP 0x80 //if SYSCLK<30MHz
//define ENABLE_IAP 0x81 //if SYSCLK<24MHz
#define ENABLE_IAP 0x82 //if SYSCLK<20MHz
//define ENABLE_IAP 0x83 //if SYSCLK<12MHz
//define ENABLE_IAP 0x84 //if SYSCLK<6MHz
//define ENABLE_IAP 0x85 //if SYSCLK<3MHz
//define ENABLE_IAP 0x86 //if SYSCLK<2MHz
//define ENABLE_IAP 0x87 //if SYSCLK<1MHz

//Start address for STC12C5A60S2 EEPROM
#define IAP_ADDRESS 0x0000

void Delay(BYTE n);
void IapIdle();
BYTE IapReadByte(WORD addr);
void IapProgramByte(WORD addr, BYTE dat);
void IapEraseSector(WORD addr);

void main()
{
    WORD i;

    P1 = 0xFE;                                               //1111,1110 System Reset OK
    Delay(10);            //Delay
    IapEraseSector(IAP_ADDRESS);        //Erase current sector
    for (i=0; i<512; i++)                             //Check whether all sector data is FF
    {
        if (IapReadByte(IAP_ADDRESS+i) != 0xff)
            goto Error;                                  //If error, break
    }
    P1 = 0xFC;                                            //1111,1100 Erase successful
    Delay(10);                                           //Delay
    for (i=0; i<512; i++)                           //Program 512 bytes data into data flash
    {
        IapProgramByte(IAP_ADDRESS+i, (BYTE)i);
    }
    P1 = 0xF8;                                        //1111,1000 Program successful
    Delay(10);                                   //Delay
    for (i=0; i<512; i++)                      //Verify 512 bytes data
    {
        if (IapReadByte(IAP_ADDRESS+i) != (BYTE)i)
            goto Error;                         //If error, break
    }
    P1 = 0xF0;                                     //1111,0000 Verify successful
    while (1);
    Error:
    P1 &= 0x7f;                             //0xxx,xxxx IAP operation fail
    while (1);
}

/*-----------------------------
Software delay function
-----------------------------*/
void Delay(BYTE n)
{
    WORD x;

    while (n--)
    {
        x = 0;
        while (++x);
    }
}
void IapIdle()
{
    IAP_CONTR = 0;  // Close IAP function
    IAP_CMD = 0;   // Clear command to standby
    IAP_TRIG = 0;  // Clear trigger register
    IAP_ADDRH = 0x80;  // Data ptr point to non-EEPROM area
    IAP_ADDRL = 0;    // Clear IAP address to prevent misuse
}

BYTE IapReadByte(WORD addr)
{
    BYTE dat;   // Data buffer
    IAP_CONTR = ENABLE_IAP;  // Open IAP function, and set wait time
    IAP_CMD = CMD_READ;   // Set ISP/IAP/EEPROM READ command
    IAP_ADDRL = addr;    // Set ISP/IAP/EEPROM address low
    IAP_ADDRH = addr >> 8;  // Set ISP/IAP/EEPROM address high
    IAP_TRIG = 0x5a;    // Send trigger command1 (0x5a)
    IAP_TRIG = 0xa5;   // Send trigger command2 (0xa5)
    _nop_();          // MCU will hold here until ISP/IAP/EEPROM
                     // operation complete
    dat = IAP_DATA;   // Read ISP/IAP/EEPROM data
    IapIdle();       // Close ISP/IAP/EEPROM function

    return dat;       // Return Flash data
}

Program one byte to ISP/IAP/EEPROM area
Input: addr (ISP/IAP/EEPROM address)
    dat (ISP/IAP/EEPROM data)
Output:
-----------------------------*/
void IapProgramByte(WORD addr, BYTE dat)
{
    IAP_CONTR = ENABLE_IAP; //Open IAP function, and set wait time
    IAP_CMD = CMD_PROGRAM; //Set ISP/IAP/EEPROM PROGRAM command
    IAP_ADDRL = addr; //Set ISP/IAP/EEPROM address low
    IAP_ADDRH = addr >> 8; //Set ISP/IAP/EEPROM address high
    IAP_DATA = dat; //Write ISP/IAP/EEPROM data
    IAP_TRIG = 0x5a; //Send trigger command1 (0x5a)
    IAP_TRIG = 0xa5; //Send trigger command2 (0xa5)
    _nop_(); //MCU will hold here until ISP/IAP/EEPROM operation complete
    IapIdle();
}

/*-----------------------------
Erase one sector area
Input: addr (ISP/IAP/EEPROM address)
Output:-
-----------------------------*/
void IapEraseSector(WORD addr)
{
    IAP_CONTR = ENABLE_IAP; //Open IAP function, and set wait time
    IAP_CMD = CMD_ERASE; //Set ISP/IAP/EEPROM ERASE command
    IAP_ADDRL = addr; //Set ISP/IAP/EEPROM address low
    IAP_ADDRH = addr >> 8; //Set ISP/IAP/EEPROM address high
    IAP_TRIG = 0x5a; //Send trigger command1 (0x5a)
    IAP_TRIG = 0xa5; //Send trigger command2 (0xa5)
    _nop_(); //MCU will hold here until ISP/IAP/EEPROM operation complete
    IapIdle();
}
Chapter 13  STC12xx series programming tools usage

13.1  In-System-Programming (ISP) principle

If need download code into STC12C5A60S2 series, P1.0 and P1.1 pin must be connected to GND. If you chose the "Next program code, P1.0/1.1 need=0/0" option, then the next time you need to re-download the program, first of all must be connected P1.0 and P1.1 to GND.

Wait ISP command for tens or hundreds milliseconds, if no legitimate command, MCU will reset to AP area.

PC application must send command at first then power on MCU.
13.2 STC12C5A60S2 series application circuit for ISP

Notes:
Traditional 8051's ALE pin regardless of whether access to external data bus, will have a clock frequency output. The signals is a source of interference to the system. For this reason, STC MCU new added a Enable/Disable ALE signal output switch, thus reduced MCU internal to external electromagnetic emissions, improve system stability and reliability. If needs the signal as other peripheral device's clock source, you can get clock source from CLKOUT0/P3.4, CLKOUT1/P3.5, CLKOUT2/P1.0 or XTAL2 clock output. (Recommended a 200ohm series resistor to the XTAL2 pin)
13.3 PC side application usage

According to actual situation, the user selects the appropriate maximum baud rate.

In practice, if P3.0/P3.1 already connected to a RS232/RS485 or other equipment, it is recommended that selection P1.0 / P1.1 = 0/0 can download options.

Press this button when mass production.

Enable the option in debugging stage.

All new settings are valid in the next power-on.
Step1: Select MCU type (E.g. STC12C5A60S2)
Step2: Load user program code (*.bin or *.hex)
Step3: Select the serial port you are using
Step4: Configure the hardware option
Step5: Press “ISP programming” or “Re-Programming” button to download user program

NOTE: Must press “ISP programming” or “Re-Programming” button first, then power on MCU, otherwise it cannot be downloaded.

About hardware connection
1. MCU RXD (P3.0) ---- RS232 ---- PC COM port TXD (Pin3)
2. MCU TXD (P3.1) ---- RS232 ---- PC COM port RXD (Pin2)
3. MCU GND -------PC COM port GND (Pin5)
4. RS232: You can select STC232 / STC3232 / MAX232 / MAX3232 / …

Using a demo board as a programmer
STC-ISP ver3.0A PCB can be welded into three kinds of circuits, respectively, support the STC's 16/20/28/32 pins MCU, the back plate of the download boards are affixed with labels, users need to pay special attention to. All the download board is welded 40-pin socket, the socket’s 20-pin is ground line, all types of MCU should be put on the socket according to the way of alignment with the ground. The method of programming user code using download board as follow:
1. According to the type of MCU choose supply voltage,
   A. For 5V MCU, using jumper JP1 to connect MCU-VCC to +5V pin
   B. For 3V MCU, using jumper JP1 to connect MCU-VCC to +3.3V pin

2. Download cable (Provided by STC)
   A. Connect DB9 serial connector to the computer's RS-232 serial interface
   B. Plug the USB interface at the same side into your computer's USB port for power supply
   C. Connect the USB interface at the other side into STC download board

3. Other interfaces do not need to connect.
4. In a non-pressed state to SW1, and MCU-VCC power LED off.
5. For SW3
   P1.0/P1.1 = 1/1 when SW3 is non-pressed
   P1.0/P1.1 = 0/0 when SW3 is pressed
   If you have select the “Next program code, P1.0/P1.1 Need = 0/0” option, then SW3 must be in a pressed state
6. Put target MCU into the U1 socket, and locking socket
7. Press the “Download” button in the PC side application
8. Press SW1 switch in the download board
9. Close the demo board power supply and remove the MCU after download successfully.
13.4 Compiler / Assembler Programmer and Emulator

About Compiler/Assembler
Any traditional compiler / assembler and the popular Keil are suitable for STC MCU. For selection MCU body, the traditional compiler / assembler, you can choose Intel's 8052 / 87C52 / 87C52 / 87C58 or Philips's P87C52 / P87C54/P87C58 in the traditional environment, in Keil environment, you can choose the types in front of the proposed or download the STC chips database file (STC.CDB) from the STC official website.

About Programmer
You can use the STC specific ISP programmer. (Can be purchased from the STC or apply for free sample). Programmer can be used as demo board

About Emulator
We do not provide specific emulator now. If you have a traditional 8051 emulator, you can use it to simulate STC MCU’s some 8052 basic functions.

13.5 Self-Defined ISP download Demo
/*-------------------------------------------------------------------------------------------------------------*/
/* --- STC MCU International Limited ------------------------------------------------------------------------*/
/* --- STC 1T Series MCU using software to custom download code Demo------------------------------------------*/
/* --- Mobile: (86)13922805190 ------------------------------------------------------------------------*/
/* --- Fax: 86-755-82944243 ----------------------------------------------------------------------------*/
/* --- Tel: 86-755-82948412 -----------------------------------------------------------------------------*/
/* --- Web: www.STCMCU.com ------------------------------------------------------------------------*/
/* If you want to use the program or the program referenced in the article, please specify in which data and procedures from STC*/
/*-------------------------------------------------------------------------------------------------------------*/
#include <reg51.h>
#include <instrins.h>

sfr IAP_CONTR = 0xc7;
sbit MCU_Start_Led = P1^7;

#define Self_Define_ISP_Download_Command 0x22
#define RELOAD_COUNT 0xfb //18.432MHz,12T,SMOD=0,9600bps
#define RELOAD_COUNT 0xf6 //18.432MHz,12T,SMOD=0,4800bps
#define RELOAD_COUNT 0xec //18.432MHz,12T,SMOD=0,2400bps
#define RELOAD_COUNT 0xd8 //18.432MHz,12T,SMOD=0,1200bps

void serial_port_initial(void);
void send_UART(unsigned char);
void UART_Interrupt_Receive(void);
void soft_reset_to_ISP_Monitor(void);
void delay(void);
void display_MCU_Start_Led(void);
void main(void)
{
    unsigned char i = 0;

    serial_port_initial(); //Initial UART
    display_MCU_Start_Led(); //Turn on the work LED
    send_UART(0x34); //Send UART test data
    send_UART(0xa7); // Send UART test data
    while (1);
}

void send_UART(unsigned char i)
{
    ES = 0; //Disable serial interrupt
    TI = 0; //Clear TI flag
    SBUF = i; //send this data
    while (!TI); //wait for the data is sent
    TI = 0; //clear TI flag
    ES = 1; //enable serial interrupt
}

void UART_Interrupt.Receive(void) interrupt 4 using 1
{
    unsigned char k = 0;
    if (RI)
    {
        RI = 0;
        k = SBUF;
        if (k == Self_Define_ISP_Command) //check the serial data
        {
            delay(); //delay 1s
            delay(); //delay 1s
            soft_reset_to_ISP_Monitor();
        }
    }
    if (TI)
    {
        TI = 0;
    }
}

void soft_reset_to_ISP_Monitor(void)
{
    IAP_CONTR = 0x60; //0110,0000 soft reset system to run ISP monitor
}
void delay(void)
{
    unsigned int j = 0;
    unsigned int g = 0;
    for (j=0; j<5; j++)
    {
        for (g=0; g<60000; g++)
        {
            _nop_();
            _nop_();
            _nop_();
            _nop_();
            _nop_();
        }
    }
}

void display_MCU_Start_Led(void)
{
    unsigned char i = 0;
    for (i=0; i<3; i++)
    {
        MCU_Start_Led = 0; //Turn on work LED
dejay();
        MCU_Start_Led = 1; //Turn off work LED
dejay();
        MCU_Start_Led = 0; //Turn on work LED
    }
}

In addition, the PC-side application also need to make the following settings

- **Baud**: 9600
- **Command (HEX)**: 22
- **Reload the file automatically if the file is changed and send the Command automatically.**

![Options and Settings](image-url)
Appendix A: Assembly Language Programming

INTRODUCTION

Assembly language is a computer language lying between the extremes of machine language and high-level language like Pascal or C use words and statements that are easily understood by humans, although still a long way from "natural" language. Machine language is the binary language of computers. A machine language program is a series of binary bytes representing instructions the computer can execute.

Assembly language replaces the binary codes of machine language with easy to remember "mnemonics" that facilitate programming. For example, an addition instruction in machine language might be represented by the code "10110011". It might be represented in assembly language by the mnemonic "ADD". Programming with mnemonics is obviously preferable to programming with binary codes.

Of course, this is not the whole story. Instructions operate on data, and the location of the data is specified by various "addressing modes" embedded in the binary code of the machine language instruction. So, there may be several variations of the ADD instruction, depending on what is added. The rules for specifying these variations are central to the theme of assembly language programming.

An assembly language program is not executable by a computer. Once written, the program must undergo translation to machine language. In the example above, the mnemonic "ADD" must be translated to the binary code "10110011". Depending on the complexity of the programming environment, this translation may involve one or more steps before an executable machine language program results. As a minimum, a program called an "assembler" is required to translate the instruction mnemonics to machine language binary codes. A further step may require a "linker" to combine portions of program from separate files and to set the address in memory at which the program may execute. We begin with a few definitions.

An assembly language program is a program written using labels, mnemonics, and so on, in which each statement corresponds to a machine instruction. Assembly language programs, often called source code or symbolic code, cannot be executed by a computer.

A machine language program is a program containing binary codes that represent instructions to a computer. Machine language programs, often called object code, are executable by a computer.

An assembler is a program that translates an assembly language program into a machine language program. The machine language program (object code) may be in "absolute" form or in "relocatable" form. In the latter case, "linking" is required to set the absolute address for execution.

A linker is a program that combines relocatable object programs (modules) and produces an absolute object program that is executable by a computer. A linker is sometimes called a "linker/locator" to reflect its separate functions of combining relocatable modules (linking) and setting the address for execution (locating).

A segment is a unit of code or data memory. A segment may be relocatable or absolute. A relocatable segment has a name, type, and other attributes that allow the linker to combine it with other partial segments, if required, and to correctly locate the segment. An absolute segment has no name and cannot be combined with other segments.

A module contains one or more segments or partial segments. A module has a name assigned by the user. The module definitions determine the scope of local symbols. An object file contains one or more modules. A module may be thought of as a "file" in many instances.

A program consists of a single absolute module, merging all absolute and relocatable segments from all input modules. A program contains only the binary codes for instructions (with address and data constants) that are understood by a computer.
ASSEMBLER OPERATION

There are many assembler programs and other support programs available to facilitate the development of applications for the 8051 microcontroller. Intel's original MCS-51 family assembler, ASM51, is no longer available commercially. However, it set the standard to which the others are compared.

ASM51 is a powerful assembler with all the bells and whistles. It is available on Intel development systems and on the IBM PC family of microcomputers. Since these "host" computers contain a CPU chip other than the 8051, ASM51 is called a cross assembler. An 8051 source program may be written on the host computer (using any text editor) and may be assembled to an object file and listing file (using ASM51), but the program may not be executed. Since the host system's CPU chip is not an 8051, it does not understand the binary instruction in the object file. Execution on the host computer requires either hardware emulation or software simulation of the target CPU. A third possibility is to download the object program to an 8051-based target system for execution.

ASM51 is invoked from the system prompt by

```
ASM51 source_file [assembler_controls]
```

The source file is assembled and any assembler controls specified take effect. The assembler receives a source file as input (e.g., PROGRAM.SRC) and generates an object file (PROGRAM.OBJ) and listing file (PROGRAM.LST) as output. This is illustrated in Figure 1.

Since most assemblers scan the source program twice in performing the translation to machine language, they are described as two-pass assemblers. The assembler uses a location counter as the address of instructions and the values for labels. The action of each pass is described below.

![Diagram of the assembly process](image)

**Legend**
- Utility program
- User file

**Figure 1** Assembling a source program

**Pass one**
During the first pass, the source file is scanned line-by-line and a symbol table is built. The location counter defaults to 0 or is set by the ORG (set origin) directive. As the file is scanned, the location counter is incremented by the length of each instruction. Define data directives (DBs or DWs) increment the location counter by the number of bytes defined. Reserve memory directives (DSs) increment the location counter by the number of bytes reserved.

Each time a label is found at the beginning of a line, it is placed in the symbol table along with the current value of the location counter. Symbols that are defined using equate directives (EQUs) are placed in the symbol table along with the "equated" value. The symbol table is saved and then used during pass two.

**Pass two**
During pass two, the object and listing files are created. Mnemonics are converted to opcodes and placed in the output files. Operands are evaluated and placed after the instruction opcodes. Where symbols appear in the operand field, their values are retrieved from the symbol table (created during pass one) and used in calculating the correct data or addresses for the instructions.

Since two passes are performed, the source program may use "forward references", that is, use a symbol before it is defined. This would occur, for example, in branching ahead in a program.
The object file, if it is absolute, contains only the binary bytes (00H-0FH) of the machine language program. A relocatable object file will also contain a symbol table and other information required for linking and locating. The listing file contains ASCII text codes (02H-7EH) for both the source program and the hexadecimal bytes in the machine language program.

A good demonstration of the distinction between an object file and a listing file is to display each on the host computer's CRT display (using, for example, the TYPE command on MS-DOS systems). The listing file clearly displays, with each line of output containing an address, opcode, and perhaps data, followed by the program statement from the source file. The listing file displays properly because it contains only ASCII text codes. Displaying the object file is a problem, however. The output will appear as "garbage", since the object file contains binary codes of an 8051 machine language program, rather than ASCII text codes.

**ASSEMBLY LANGUAGE PROGRAM FORMAT**

Assembly language programs contain the following:

- Machine instructions
- Assembler directives
- Assembler controls
- Comments

Machine instructions are the familiar mnemonics of executable instructions (e.g., ANL). Assembler directives are instructions to the assembler program that define program structure, symbols, data, constants, and so on (e.g., ORG). Assembler controls set assembler modes and direct assembly flow (e.g., STITLE). Comments enhance the readability of programs by explaining the purpose and operation of instruction sequences.

Those lines containing machine instructions or assembler directives must be written following specific rules understood by the assembler. Each line is divided into "fields" separated by space or tab characters. The general format for each line is as follows:

```
[label:] mnemonic [operand] [, operand] […] ;comment
```

Only the mnemonic field is mandatory. Many assemblers require the label field, if present, to begin on the left in column 1, and subsequent fields to be separated by space or tab characters. With ASM51, the label field needn't begin in column 1 and the mnemonic field needn't be on the same line as the label field. The operand field must, however, begin on the same line as the mnemonic field. The fields are described below.

**Label Field**

A label represents the address of the instruction (or data) that follows. When branching to this instruction, this label is used in the operand field of the branch or jump instruction (e.g., SJMP SKIP).

Whereas the term "label" always represents an address, the term "symbol" is more general. Labels are one type of symbol and are identified by the requirement that they must terminate with a colon (\(:)\). Symbols are assigned values or attributes, using directives such as EQU, SEGMENT, BIT, DATA, etc. Symbols may be addresses, data constants, names of segments, or other constructs conceived by the programmer. Symbols do not terminate with a colon. In the example below, PAR is a symbol and START is a label (which is a type of symbol).

```
PAR EQU 500 ;"PAR" IS A SYMBOL WHICH
;REPRESENTS THE VALUE 500

START: MOV A,#0FFH ;"START" IS A LABEL WHICH
;REPRESENTS THE ADDRESS OF
;THE MOV INSTRUCTION
```

A symbol (or label) must begin with a letter, question mark, or underscore (_); must be followed by letters, digit, "?", or ";"; and can contain up to 31 characters. Symbols may use upper- or lowercase characters, but they are treated the same. Reserved words (mnemonics, operators, predefined symbols, and directives) may not be used.
Mnemonic Field
Instruction mnemonics or assembler directives go into mnemonic field, which follows the label field. Examples of instruction mnemonics are ADD, MOV, DIV, or INC. Examples of assembler directives are ORG, EQU, or DB.

Operand Field
The operand field follows the mnemonic field. This field contains the address or data used by the instruction. A label may be used to represent the address of the data, or a symbol may be used to represent a data constant. The possibilities for the operand field are largely dependent on the operation. Some operations have no operand (e.g., the RET instruction), while others allow for multiple operands separated by commas. Indeed, the possibilities for the operand field are numerous, and we shall elaborate on these at length. But first, the comment field.

Comment Field
Remarks to clarify the program go into comment field at the end of each line. Comments must begin with a semicolon (;). Each lines may be comment lines by beginning them with a semicolon. Subroutines and large sections of a program generally begin with a comment block—serveral lines of comments that explain the general properties of the section of software that follows.

Special Assembler Symbols
Special assembler symbols are used for the register-specific addressing modes. These include A, R0 through R7, DPTR, PC, C and AB. In addition, a dollar sign ($) can be used to refer to the current value of the location counter. Some examples follow.

\begin{verbatim}
SETB C
INC DPTR
JNB TI, $
\end{verbatim}

The last instruction above makes effective use of ASM51's location counter to avoid using a label. It could also be written as

\begin{verbatim}
HERE: JNB TI, HERE
\end{verbatim}

Indirect Address
For certain instructions, the operand field may specify a register that contains the address of the data. The commercial "at" sign (@) indicates address indirection and may only be used with R0, R1, the DPTR, or the PC, depending on the instruction. For example,

\begin{verbatim}
ADD A, @R0
MOVC A, @A+PC
\end{verbatim}

The first instruction above retrieves a byte of data from internal RAM at the address specified in R0. The second instruction retrieves a byte of data from external code memory at the address formed by adding the contents of the accumulator to the program counter. Note that the value of the program counter, when the add takes place, is the address of the instruction following MOVC. For both instruction above, the value retrieved is placed into the accumulator.

Immediate Data
Instructions using immediate addressing provide data in the operand field that become part of the instruction. Immediate data are preceded with a pound sign (#). For example,
CONSTANT EQU 100
MOV A, #0FEH
ORL 40H, #CONSTANT

All immediate data operations (except MOV DPTR,#data) require eight bits of data. The immediate data are evaluated as a 16-bit constant, and then the low-byte is used. All bits in the high-byte must be the same (00H or FFH) or the error message "value will not fit in a byte" is generated. For example, the following instructions are syntactically correct:

MOV A, #0FF00H
MOV A, #00FFH

But the following two instructions generate error messages:

MOV A, #0FE00H
MOV A, #01FFH

If signed decimal notation is used, constants from -256 to +255 may also be used. For example, the following two instructions are equivalent (and syntactically correct):

MOV A, #-256
MOV A, #0FF00H

Both instructions above put 00H into accumulator A.

Data Address

Many instructions access memory locations using direct addressing and require an on-chip data memory address (00H to 7FH) or an SFR address (80H to 0FFH) in the operand field. Predefined symbols may be used for the SFR addresses. For example,

MOV A, 45H
MOV A, SBUF ;SAME AS MOV A, 99H

Bit Address

One of the most powerful features of the 8051 is the ability to access individual bits without the need for masking operations on bytes. Instructions accessing bit-addressable locations must provide a bit address in internal data memory (00h to 7FH) or a bit address in the SFRs (80H to 0FFH).

There are three ways to specify a bit address in an instruction: (a) explicitly by giving the address, (b) using the dot operator between the byte address and the bit position, and (c) using a predefined assembler symbol. Some examples follow.

SETB 0E7H ;EXPLICIT BIT ADDRESS
SETB ACC.7 ;DOT OPERATOR (SAME AS ABOVE)
JNB TI, $ ;"TI" IS A PRE-DEFINED SYMBOL
JNB 99H, $ ;(SAME AS ABOVE)

Code Address

A code address is used in the operand field for jump instructions, including relative jumps (SJMP and conditional jumps), absolute jumps and calls (ACALL, AJMP), and long jumps and calls (LJMP, LCALL).

The code address is usually given in the form of a label.

ASM51 will determine the correct code address and insert into the instruction the correct 8-bit signed offset, 11-bit page address, or 16-bit long address, as appropriate.
Generic Jumps and Calls

ASM51 allows programmers to use a generic JMP or CALL mnemonic. "JMP" can be used instead of SJMP, AJMP or LJMP; and "CALL" can be used instead of ACALL or LCALL. The assembler converts the generic mnemonic to a "real" instruction following a few simple rules. The generic mnemonic converts to the short form (for JMP only) if no forward references are used and the jump destination is within -128 locations, or to the absolute form if no forward references are used and the instruction following the JMP or CALL instruction is in the same 2K block as the destination instruction. If short or absolute forms cannot be used, the conversion is to the long form.

The conversion is not necessarily the best programming choice. For example, if branching ahead a few instructions, the generic JMP will always convert to LJMP even though an SJMP is probably better. Consider the following assembled instructions sequence using three generic jumps.

<table>
<thead>
<tr>
<th>LOC</th>
<th>OBJ</th>
<th>LINE</th>
<th>SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1234</td>
<td>04</td>
<td>2</td>
<td>START: INC A</td>
</tr>
<tr>
<td>1234</td>
<td>04</td>
<td>3</td>
<td>JMP START ;ASSEMBLES AS SJMP</td>
</tr>
<tr>
<td>1235</td>
<td>0F</td>
<td>4</td>
<td>ORG START + 200</td>
</tr>
<tr>
<td>12FC</td>
<td>41</td>
<td>5</td>
<td>JMP START ;ASSEMBLES AS AJMP</td>
</tr>
<tr>
<td>12FC</td>
<td>02</td>
<td>6</td>
<td>JMP FINISH ;ASSEMBLES AS LJMP</td>
</tr>
<tr>
<td>1301</td>
<td>04</td>
<td>7</td>
<td>FINISH: INC A</td>
</tr>
<tr>
<td>1304</td>
<td>04</td>
<td>8</td>
<td>END</td>
</tr>
</tbody>
</table>

The first jump (line 3) assembles as SJMP because the destination is before the jump (i.e., no forward reference) and the offset is less than -128. The ORG directive in line 4 creates a gap of 200 locations between the label START and the second jump, so the conversion on line 5 is to AJMP because the offset is too great for SJMP. Note also that the address following the second jump (12FEH) and the address of START (1234H) are within the same 2K page, which, for this instruction sequence, is bounded by 1000H and 17FFH. This criterion must be met for absolute addressing. The third jump assembles as LJMP because the destination (FINISH) is not yet defined when the jump is assembled (i.e., a forward reference is used). The reader can verify that the conversion is as stated by examining the object field for each jump instruction.

ASSEMBLE-TIME EXPRESSION EVALUATION

Values and constants in the operand field may be expressed three ways: (a) explicitly (e.g., 0EFH), (b) with a predefined symbol (e.g., ACC), or (c) with an expression (e.g., 2 + 3). The use of expressions provides a powerful technique for making assembly language programs more readable and more flexible. When an expression is used, the assembler calculates a value and inserts it into the instruction.

All expression calculations are performed using 16-bit arithmetic; however, either 8 or 16 bits are inserted into the instruction as needed. For example, the following two instructions are the same:

MOV DPTR, #04FFH + 3
MOV DPTR, #0502H ;ENTIRE 16-BIT RESULT USED

If the same expression is used in a "MOV A,#data" instruction, however, the error message "value will not fit in a byte" is generated by ASM51. An overview of the rules for evaluating expressions follows.
Number Bases
The base for numeric constants is indicated in the usual way for Intel microprocessors. Constants must be followed with "B" for binary, "O" or "Q" for octal, "D" or nothing for decimal, or "H" for hexadecimal. For example, the following instructions are the same:

```
MOV   A, #15H
MOV   A, #1111B
MOV   A, #0FH
MOV   A, #17Q
MOV   A, #15D
```

Note that a digit must be the first character for hexadecimal constants in order to differentiate them from labels (i.e., "0A5H" not "A5H").

Character Strings
Strings using one or two characters may be used as operands in expressions. The ASCII codes are converted to the binary equivalent by the assembler. Character constants are enclosed in single quotes ('). Some examples follow.

```
CJNE   A, # 'Q', AGAIN
SUBB   A, # '0'   ;CONVERT ASCII DIGIT TO BINARY DIGIT
MOV    DPTR, # 'AB'
MOV    DPTR, #4142H  ;SAME AS ABOVE
```

Arithmetic Operators
The arithmetic operators are

+ addition
- subtraction
* multiplication
/ division
MOD modulo (remainder after division)

For example, the following two instructions are same:

```
MOV   A, 10 +10H
MOV   A, #1AH
```

The following two instructions are also the same:

```
MOV   A, #25 MOD 7
MOV   A, #4
```

Since the MOD operator could be confused with a symbol, it must be separated from its operands by at least one space or tab character, or the operands must be enclosed in parentheses. The same applies for the other operators composed of letters.

Logical Operators
The logical operators are

OR logical OR
AND logical AND
XOR logical Exclusive OR
NOT logical NOT (complement)
The operation is applied on the corresponding bits in each operand. The operator must be separated from the operands by space or tab characters. For example, the following two instructions are the same:

```
MOV A, # '9' AND 0FH
MOV A, #9
```

The NOT operator only takes one operand. The following three MOV instructions are the same:

```
THREE EQU 3
MINUS_THREE EQU -3
MOV A, # (NOT THREE) + 1
MOV A, #MINUS_THREE
MOV A, #11111101B
```

### Special Operators

The special operators are

- **SHR** shift right
- **SHL** shift left
- **HIGH** high-byte
- **LOW** low-byte
- **()** evaluate first

For example, the following two instructions are the same:

```
MOV A, #8 SHL 1
MOV A, #10H
```

The following two instructions are also the same:

```
MOV A, #HIGH 1234H
MOV A, #12H
```

### Relational Operators

When a relational operator is used between two operands, the result is always false (0000H) or true (FFFFH). The operators are

- **EQ** = equals
- **NE** <> not equals
- **LT** < less than
- **LE** <= less than or equal to
- **GT** > greater than
- **GE** >= greater than or equal to

Note that for each operator, two forms are acceptable (e.g., "EQ" or "="). In the following examples, all relational tests are "true":

```
MOV A, #5 = 5
MOV A, #5 NE 4
MOV A, #'X' LT #'Z'
MOV A, #'X' GE #'X'
MOV A, #$ > 0
MOV A, #100 GE 50
```
So, the assembled instructions are equal to

```
MOV   A, #0FFH
```

Even though expressions evaluate to 16-bit results (i.e., 0FFFFH), in the examples above only the low-order eight bits are used, since the instruction is a move byte operation. The result is not considered too big in this case, because as signed numbers the 16-bit value FFFFH and the 8-bit value FFH are the same (-1).

**Expression Examples**

The following are examples of expressions and the values that result:

<table>
<thead>
<tr>
<th>Expression</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>'B' - 'A'</td>
<td>0001H</td>
</tr>
<tr>
<td>8/3</td>
<td>0002H</td>
</tr>
<tr>
<td>155 MOD 2</td>
<td>0001H</td>
</tr>
<tr>
<td>4 * 4</td>
<td>0010H</td>
</tr>
<tr>
<td>8 AND 7</td>
<td>0000H</td>
</tr>
<tr>
<td>NOT 1</td>
<td>FFFEH</td>
</tr>
<tr>
<td>'A' SHL 8</td>
<td>4100H</td>
</tr>
<tr>
<td>LOW 65535</td>
<td>00FFH</td>
</tr>
<tr>
<td>(8 + 1) * 2</td>
<td>0012H</td>
</tr>
<tr>
<td>5 EQ 4</td>
<td>0000H</td>
</tr>
<tr>
<td>'A' LT 'B'</td>
<td>FFFFH</td>
</tr>
<tr>
<td>3 &lt;= 3</td>
<td>FFFFHs</td>
</tr>
</tbody>
</table>

A practical example that illustrates a common operation for timer initialization follows: Put -500 into Timer 1 registers TH1 and TL1. In using the HIGH and LOW operators, a good approach is

```
VALUE EQU -500
MOV   TH1, #HIGH VALUE
MOV   TL1, #LOW VALUE
```

The assembler converts -500 to the corresponding 16-bit value (FE0CH); then the HIGH and LOW operators extract the high (FEH) and low (0CH) bytes, as appropriate for each MOV instruction.

**Operator Precedence**

The precedence of expression operators from highest to lowest is

```
()  \nHIGH LOW \n* / MOD SHL SHR \n+ - \nEQ NE LT LE GT GE = <> <= => \nNOT \nAND \nOR XOR
```

When operators of the same precedence are used, they are evaluated left to right.

**Examples:**

<table>
<thead>
<tr>
<th>Expression</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIGH ('A' SHL 8)</td>
<td>0041H</td>
</tr>
<tr>
<td>HIGH 'A' SHL 8</td>
<td>0000H</td>
</tr>
<tr>
<td>NOT 'A' - 1</td>
<td>FFBFH</td>
</tr>
<tr>
<td>'A' OR 'A' SHL 8</td>
<td>4141H</td>
</tr>
</tbody>
</table>
ASSEMBLER DIRECTIVES

Assembler directives are instructions to the assembler program. They are not assembly language instructions executable by the target microprocessor. However, they are placed in the mnemonic field of the program. With the exception of DB and DW, they have no direct effect on the contents of memory.

ASM51 provides several categories of directives:

- Assembler state control (ORG, END, USING)
- Symbol definition (SEGMENT, EQU, SET, DATA, IDATA, XDATA, BIT, CODE)
- Storage initialization/reservation (DS, DBIT, DB, DW)
- Program linkage (PUBLIC, EXTRN, NAME)
- Segment selection (RSEG, CSEG, DSEG, ISEG, ESEG, XSEG)

Each assembler directive is presented below, ordered by category.

Assembler State Control

**ORG (Set Origin)**

The format for the ORG (set origin) directive is

```
ORG expression
```

The ORG directive alters the location counter to set a new program origin for statements that follow. A label is not permitted. Two examples follow.

```
ORG 100H ;SET LOCATION COUNTER TO 100H
ORG ($ + 1000H) AND 0F00H ;SET TO NEXT 4K BOUNDARY
```

The ORG directive can be used in any segment type. If the current segment is absolute, the value will be an absolute address in the current segment. If a relocatable segment is active, the value of the ORG expression is treated as an offset from the base address of the current instance of the segment.

**END**

The format of the END directive is

```
END
```

END should be the last statement in the source file. No label is permitted and nothing beyond the END statement is processed by the assembler.

**Using**

The format of the END directive is

```
USING expression
```

This directive informs ASM51 of the currently active register bank. Subsequent uses of the predefined symbolic register addresses AR0 to AR7 will convert to the appropriate direct address for the active register bank. Consider the following sequence:

```
USING 3
PUSH AR7
USING 1
PUSH AR7
```

The first push above assembles to PUSH 1FH (R7 in bank 3), whereas the second push assembles to PUSH 0FH (R7 in bank 1).

Note that USING does not actually switch register banks; it only informs ASM51 of the active bank. Executing 8051 instructions is the only way to switch register banks. This is illustrated by modifying the example above as follows:
Symbol Definition

The symbol definition directives create symbols that represent segment, registers, numbers, and addresses. None of these directives may be preceded by a label. Symbols defined by these directives may not have been previously defined and may not be redefined by any means. The SET directive is the only exception. Symbol definition directives are described below.

Segment

The format for the SEGMENT directive is shown below.

symbol SEGMENT segment_type

The symbol is the name of a relocatable segment. In the use of segments, ASM51 is more complex than conventional assemblers, which generally support only "code" and "data" segment types. However, ASM51 defines additional segment types to accommodate the diverse memory spaces in the 8051. The following are the defined 8051 segment types (memory spaces):

- CODE (the code segment)
- XDATA (the external data space)
- DATA (the internal data space accessible by direct addressing, 00H–07H)
- IDATA (the entire internal data space accessible by indirect addressing, 00H–07H)
- BIT (the bit space; overlapping byte locations 20H–2FH of the internal data space)

For example, the statement

EPROM SEGMENT CODE

declares the symbol EPROM to be a SEGMENT of type CODE. Note that this statement simply declares what EPROM is. To actually begin using this segment, the RSEG directive is used (see below).

EQU (Equate)

The format for the EQU directive is

Symbol EQU expression

The EQU directive assigns a numeric value to a specified symbol name. The symbol must be a valid symbol name, and the expression must conform to the rules described earlier.

The following are examples of the EQU directive:

N27 EQU 27 ;SET N27 TO THE VALUE 27
HERE EQU $ ;SET "HERE" TO THE VALUE OF
;THE LOCATION COUNTER
CR EQU 0DH ;SET CR (CARRIAGE RETURN) TO 0DH
MESSAGE: DB 'This is a message'
LENGTH EQU $ - MESSAGE ;"LENGTH" EQUALS LENGTH OF "MESSAGE"

Other Symbol Definition Directives

The SET directive is similar to the EQU directive except the symbol may be redefined later, using another SET directive.
The DATA, IDATA, XDATA, BIT, and CODE directives assign addresses of the corresponding segment type to a symbol. These directives are not essential. A similar effect can be achieved using the EQU directive; if used, however, they evoke powerful type-checking by ASM51. Consider the following two directives and four instructions:

```
FLAG1  EQU 05H
FLAG2  BIT  05H
SETB FLAG1
SETB FLAG2
MOV  FLAG1, #0
MOV  FLAG2, #0
```

The use of FLAG2 in the last instruction in this sequence will generate a "data segment address expected" error message from ASM51. Since FLAG2 is defined as a bit address (using the BIT directive), it can be used in a set bit instruction, but it cannot be used in a move byte instruction. Hence, the error. Even though FLAG1 represents the same value (05H), it was defined using EQU and does not have an associated address space. This is not an advantage of EQU, but rather, a disadvantage. By properly defining address symbols for use in a specific memory space (using the directives BIT, DATA, XDATA, etc.), the programmer takes advantage of ASM51's powerful type-checking and avoids bugs from the misuse of symbols.

**Storage Initialization/Reservation**

The storage initialization and reservation directives initialize and reserve space in either word, byte, or bit units. The space reserved starts at the location indicated by the current value of the location counter in the currently active segment. These directives may be preceded by a label. The storage initialization/reservation directives are described below.

**DS (Define Storage)**

The format for the DS (define storage) directive is

```
[label:]  DS expression
```

The DS directive reserves space in byte units. It can be used in any segment type except BIT. The expression must be a valid assemble-time expression with no forward references and no relocatable or external references. When a DS statement is encountered in a program, the location counter of the current segment is incremented by the value of the expression. The sum of the location counter and the specified expression should not exceed the limitations of the current address space.

The following statement create a 40-byte buffer in the internal data segment:

```
DSEG  AT  30H ;PUT IN DATA SEGMENT (ABSOLUTE, INTERNAL)
LENGTH EQU 40
BUFFER: DS LENGRH ;40 BYTES RESERVED
```

The label BUFFER represents the address of the first location of reserved memory. For this example, the buffer begins at address 30H because "AT 30H" is specified with DSEG. The buffer could be cleared using the following instruction sequence:

```
MOV  R7, #LENGTH
MOV  R0, #BUFFER
LOOP: MOV  @R0, #0
DJNZ R7, LOOP
```

(continue)
To create a 1000-byte buffer in external RAM starting at 4000H, the following directives could be used:

```
XSTART   EQU 4000H
XLENGTH  EQU 1000
XSEG     AT XSTART
XBUFFER: DS XLENGTH
```

This buffer could be cleared with the following instruction sequence:

```
MOV     DPTR, #XBUFFER
LOOP:   CLR    A
        MOVX    @DPTR, A
        INC    DPTR
        MOV     A, DPL
        CJNE    A, #LOW (XBUFFER + XLENGTH + 1), LOOP
        MOV     A, DPH
        CJNE    A, #HIGH (XBUFFER + XLENGTH + 1), LOOP
```

This is an excellent example of a powerful use of ASM51's operators and assemble-time expressions. Since an instruction does not exist to compare the data pointer with an immediate value, the operation must be fabricated from available instructions. Two compares are required, one each for the high- and low-bytes of the DPTR. Furthermore, the compare-and-jump-if-not-equal instruction works only with the accumulator or a register, so the data pointer bytes must be moved into the accumulator before the CJNE instruction. The loop terminates only when the data pointer has reached XBUFFER + LENGTH + 1. (The "+1" is needed because the data pointer is incremented after the last MOVX instruction.)

**DBIT**

The format for the DBIT (define bit) directive is,

```
[label:]  DBIT  expression
```

The DBIT directive reserves space in bit units. It can be used only in a BIT segment. The expression must be a valid assemble-time expression with no forward references. When the DBIT statement is encountered in a program, the location counter of the current (BIT) segment is incremented by the value of the expression. Note that in a BIT segment, the basic unit of the location counter is bits rather than bytes. The following directives creat three flags in a absolute bit segment:

```
BSEG ;BIT SEGMENT (ABSOLUTE)
KEFLAG: DBIT 1 ;KEYBOARD STATUS
PRFLAG: DBIT 1 ;PRINTER STATUS
DKFLAG: DBIT 1 ;DISK STATUS
```

Since an address is not specified with BSEG in the example above, the address of the flags defined by DBIT could be determined (if one wishes to to so) by examining the symbol table in the .LST or .M51 files. If the definitions above were the first use of BSEG, then KBFLAG would be at bit address 00H (bit 0 of byte address 20H). If other bits were defined previously using BSEG, then the definitions above would follow the last bit defined.

**DB (Define Byte)**

The format for the DB (define byte) directive is,

```
[label:]  DB  expression [, expression] [...]
```

The DB directive initializes code memory with byte values. Since it is used to actually place data constants in code memory, a CODE segment must be active. The expression list is a series of one or more byte values (each of which may be an expression) separated by commas.
The DB directive permits character strings (enclosed in single quotes) longer than two characters as long as they are not part of an expression. Each character in the string is converted to the corresponding ASCII code. If a label is used, it is assigned the address of the first byte. For example, the following statements

```Assembly
CSEG AT 0100H
SQUARES: DB 0, 1, 4, 9, 16, 25 ; SQUARES OF NUMBERS 0-5
MESSAGE: DB 'Login:', 0 ; NULL-TERMINATED CHARACTER STRING
```

When assembled, result in the following hexadecimal memory assignments for external code memory:

<table>
<thead>
<tr>
<th>Address</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0100</td>
<td>00</td>
</tr>
<tr>
<td>0101</td>
<td>01</td>
</tr>
<tr>
<td>0102</td>
<td>04</td>
</tr>
<tr>
<td>0103</td>
<td>09</td>
</tr>
<tr>
<td>0104</td>
<td>10</td>
</tr>
<tr>
<td>0105</td>
<td>19</td>
</tr>
<tr>
<td>0106</td>
<td>4C</td>
</tr>
<tr>
<td>0107</td>
<td>6F</td>
</tr>
<tr>
<td>0108</td>
<td>67</td>
</tr>
<tr>
<td>0109</td>
<td>69</td>
</tr>
<tr>
<td>010A</td>
<td>6E</td>
</tr>
<tr>
<td>010B</td>
<td>3A</td>
</tr>
<tr>
<td>010C</td>
<td>00</td>
</tr>
</tbody>
</table>

**DW (Define Word)**

The format for the DW (define word) directive is:

```
[label:] DW expression [, expression] […]
```

The DW directive is the same as the DB directive except two memory locations (16 bits) are assigned for each data item. For example, the statements

```Assembly
CSEG AT 200H
DW $, 'A', 1234H, 2, 'BC'
```

result in the following hexadecimal memory assignments:

<table>
<thead>
<tr>
<th>Address</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0200</td>
<td>02</td>
</tr>
<tr>
<td>0201</td>
<td>00</td>
</tr>
<tr>
<td>0202</td>
<td>00</td>
</tr>
<tr>
<td>0203</td>
<td>41</td>
</tr>
<tr>
<td>0204</td>
<td>12</td>
</tr>
<tr>
<td>0205</td>
<td>34</td>
</tr>
<tr>
<td>0206</td>
<td>00</td>
</tr>
<tr>
<td>0207</td>
<td>02</td>
</tr>
<tr>
<td>0208</td>
<td>42</td>
</tr>
<tr>
<td>0209</td>
<td>43</td>
</tr>
</tbody>
</table>

**Program Linkage**

Program linkage directives allow the separately assembled modules (files) to communicate by permitting intermodule references and the naming of modules. In the following discussion, a "module" can be considered a "file." (In fact, a module may encompass more than one file.)
The format for the PUBLIC (public symbol) directive is:

PUBLIC symbol [, symbol] […]

The PUBLIC directive allows the list of specified symbols to be known and used outside the currently assembled module. A symbol declared PUBLIC must be defined in the current module. Declaring it PUBLIC allows it to be referenced in another module. For example,

PUBLIC INCHAR, OUTCHR, INLINE, OUTSTR

The format for the EXTRN (external symbol) directive is:

EXTRN segment_type (symbol [, symbol] […], …)

The EXTRN directive lists symbols to be referenced in the current module that are defined in other modules. The list of external symbols must have a segment type associated with each symbol in the list. (The segment types are CODE, XDATA, DATA, IDATA, BIT, and NUMBER. NUMBER is a type-less symbol defined by EQU.) The segment type indicates the way a symbol may be used. The information is important at link-time to ensure symbols are used properly in different modules.

The PUBLIC and EXTRN directives work together. Consider the two files, MAIN.SRC and MESSAGES.SRC. The subroutines HELLO and GOOD(ByVal are defined in the module MESSAGES but are made available to other modules using the PUBLIC directive. The subroutines are called in the module MAIN even though they are not defined there. The EXTRN directive declares that these symbols are defined in another module.

MAIN.SRC:

EXTRN CODE (HELLO, GOOD(ByVal

CALL HELLO

CALL GOOD(ByVal

END

MESSAGES.SRC:

PUBLIC HELLO, GOOD(ByVal

HELLO: (begin subroutine)

RET

GOOD(ByVal: (begin subroutine)

RET

END

Neither MAIN.SRC nor MESSAGES.SRC is a complete program; they must be assembled separately and linked together to form an executable program. During linking, the external references are resolved with correct addresses inserted as the destination for the CALL instructions.

The format for the NAME directive is:

NAME module_name
All the usual rules for symbol names apply to module names. If a name is not provided, the module takes on the file name (without a drive or subdirectory specifier and without an extension). In the absence of any use of the NAME directive, a program will contain one module for each file. The concept of "modules," therefore, is somewhat cumbersome, at least for relatively small programming problems. Even programs of moderate size (encompassing, for example, several files complete with relocatable segments) needn't use the NAME directive and needn't pay any special attention to the concept of "modules." For this reason, it was mentioned in the definition that a module may be considered a "file," to simplify learning ASM51. However, for very large programs (several thousand lines of code, or more), it makes sense to partition the problem into modules, where, for example, each module may encompass several files containing routines having a common purpose.

Segment Selection Directives

When the assembler encounters a segment selection directive, it diverts the following code or data into the selected segment until another segment is selected by a segment selection directive. The directive may select a previously defined relocatable segment or optionally create and select absolute segments.

RSEG (Relocatable Segment)  The format for the RSEG (relocatable segment) directive is

\[ \text{RSEG \hspace{1em} \text{segment\_name}} \]

Where "segment\_name" is the name of a relocatable segment previously defined with the SEGMENT directive. RSEG is a "segment selection" directive that diverts subsequent code or data into the named segment until another segment selection directive is encountered.

Selecting Absolute Segments  RSEG selects a relocatable segment. An "absolute" segment, on the other hand, is selected using one of the directives:

\[ \begin{align*}
\text{CSEG \hspace{1em} (AT \hspace{1em} \text{address})} \\
\text{DSEG \hspace{1em} (AT \hspace{1em} \text{address})} \\
\text{ISEG \hspace{1em} (AT \hspace{1em} \text{address})} \\
\text{BSEG \hspace{1em} (AT \hspace{1em} \text{address})} \\
\text{XSEG \hspace{1em} (AT \hspace{1em} \text{address})}
\end{align*} \]

These directives select an absolute segment within the code, internal data, indirect internal data, bit, or external data address spaces, respectively. If an absolute address is provided (by indicating "AT address"), the assembler terminates the last absolute address segment, if any, of the specified segment type and creates a new absolute segment starting at that address. If an absolute address is not specified, the last absolute segment of the specified type is continued. If no absolute segment of this type was previously selected and the absolute address is omitted, a new segment is created starting at location 0. Forward references are not allowed and start addresses must be absolute.

Each segment has its own location counter, which is always set to 0 initially. The default segment is an absolute code segment; therefore, the initial state of the assembler is location 0000H in the absolute code segment. When another segment is chosen for the first time, the location counter of the former segment retains the last active value. When that former segment is reselected, the location counter picks up at the last active value. The ORG directive may be used to change the location counter within the currently selected segment.

ASSEMBLER CONTROLS

Assembler controls establish the format of the listing and object files by regulating the actions of ASM51. For the most part, assembler controls affect the look of the listing file, without having any affect on the program itself. They can be entered on the invocation line when a program is assembled, or they can be placed in the source file. Assembler controls appearing in the source file must be preceded with a dollar sign and must begin in column 1.
There are two categories of assembler controls: primary and general. Primary controls can be placed in the invocation line or at the beginnig of the source program. Only other primary controls may precede a primary control. General controls may be placed anywhere in the source program.

**LINKER OPERATION**

In developing large application programs, it is common to divide tasks into subprograms or modules containing sections of code (usually subroutines) that can be written separately from the overall program. The term "modular programming" refers to this programming strategy. Generally, modules are relocatable, meaning they are not intended for a specific address in the code or data space. A linking and locating program is needed to combine the modules into one absolute object module that can be executed.

Intel's RL51 is a typical linker/locator. It processes a series of relocatable object modules as input and creates an executable machine language program (PROGRAM, perhaps) and a listing file containing a memory map and symbol table (PROGRAM.M51). This is illustrated in following figure.

As relocatable modules are combined, all values for external symbols are resolved with values inserted into the output file. The linker is invoked from the system prompt by

```
RL51 input_list  [TO output_file]  [location_controls]
```

The input_list is a list of relocatable object modules (files) separated by commas. The output_list is the name of the output absolute object module. If none is supplied, it defaults to the name of the first input file without any suffix. The location Controls set start addresses for the named segments.

For example, suppose three modules or files (MAIN.OBJ, MESSAGES.OBJ, and SUBROUTINES.OBJ) are to be combined into an executable program (EXAMPLE), and that these modules each contain two relocatable segments, one called EPROM of type CODE, and the other called ONCHIP of type DATA. Suppose further that the code segment is to be executable at address 4000H and the data segment is to reside starting at address 30H (in internal RAM). The following linker invocation could be used:

```
RS51 MAIN.OBJ,MESSAGES.OBJ,SUBROUTINES.OBJ TO EXAMPLE & CODE
(EPROM (4000H) DATA (ONCHIP (30H))
```

Note that the ampersand character "&" is used as the line continuation character.

If the program begins at the label START, and this is the first instruction in the MAIN module, then execution begins at address 4000H. If the MAIN module was not linked first, or if the label START is not at the beginning of MAIN, then the program's entry point can be determined by examining the symbol table in the listing file EXAMPLE.M51 created by RL51. By default, EXAMPLE.M51 will contain only the link map. If a symbol table is desired, then each source program must have used the SDEBUG control. The following table shows the assembler controls supported by ASM51.
## Assembler controls supported by ASM51

<table>
<thead>
<tr>
<th>Name</th>
<th>Primary/General</th>
<th>Default</th>
<th>Abbrev.</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DATE (date)</strong></td>
<td>P</td>
<td>DATE( )</td>
<td>DA</td>
<td>Place string in header (9 char. max.)</td>
</tr>
<tr>
<td><strong>DEBUG</strong></td>
<td>P</td>
<td>NODEBUG</td>
<td>DB</td>
<td>Outputs debug symbol information to object file</td>
</tr>
<tr>
<td><strong>EJECT</strong></td>
<td>G</td>
<td>not applicable</td>
<td>EJ</td>
<td>Continue listing on next page</td>
</tr>
<tr>
<td><strong>ERRORPRINT (file)</strong></td>
<td>P</td>
<td>NOERRORPRINT</td>
<td>EP</td>
<td>Designates a file to receive error messages in addition to the listing file (defaults to console)</td>
</tr>
<tr>
<td><strong>NOERRORPRINT</strong></td>
<td>P</td>
<td>NOERRORPRINT</td>
<td>NOEP</td>
<td>Designates that error messages will be printed in listing file only</td>
</tr>
<tr>
<td><strong>GEN</strong></td>
<td>G</td>
<td>GENONLY</td>
<td>GO</td>
<td>List only the fully expanded source as if all lines generated by a macro call were already in the source file</td>
</tr>
<tr>
<td><strong>GENONLY</strong></td>
<td>G</td>
<td>GENONLY</td>
<td>NOGE</td>
<td>List only the original source text in the listing file</td>
</tr>
<tr>
<td><strong>INCLUDED( file)</strong></td>
<td>G</td>
<td>not applicable</td>
<td>IC</td>
<td>Designates a file to be included as part of the program</td>
</tr>
<tr>
<td><strong>LIST</strong></td>
<td>G</td>
<td>LIST</td>
<td>LI</td>
<td>Print subsequent lines of source code in listing file</td>
</tr>
<tr>
<td><strong>NOLIST</strong></td>
<td>G</td>
<td>LIST</td>
<td>NOLI</td>
<td>Do not print subsequent lines of source code in listing file</td>
</tr>
<tr>
<td><strong>MACRO ( men_percent)</strong></td>
<td>P</td>
<td>MACRO( 50)</td>
<td>MR</td>
<td>Evaluate and expand all macro calls. Allocate percentage of free memory for macro processing</td>
</tr>
<tr>
<td><strong>NOMACRO</strong></td>
<td>P</td>
<td>MACRO( 50)</td>
<td>NOMR</td>
<td>Do not evaluate macro calls</td>
</tr>
<tr>
<td><strong>MOD51</strong></td>
<td>P</td>
<td>MOD51</td>
<td>MO</td>
<td>Recognize the 8051-specific predefined special function registers</td>
</tr>
<tr>
<td><strong>NOMOD51</strong></td>
<td>P</td>
<td>MOD51</td>
<td>NMO</td>
<td>Do not recognize the 8051-specific predefined special function registers</td>
</tr>
<tr>
<td><strong>OBJECT( file)</strong></td>
<td>P</td>
<td>OBJECT(source.OBJ)</td>
<td>OJ</td>
<td>Designates file to receive object code</td>
</tr>
<tr>
<td><strong>NOOBJECT</strong></td>
<td>P</td>
<td>OBJECT(source.OBJ)</td>
<td>NOOJ</td>
<td>Designates that no object file will be created</td>
</tr>
<tr>
<td><strong>PAGING</strong></td>
<td>P</td>
<td>PAGING</td>
<td>PI</td>
<td>Designates that listing file be broken into pages and each will have a header</td>
</tr>
<tr>
<td><strong>NOPAGING</strong></td>
<td>P</td>
<td>PAGING</td>
<td>NOPI</td>
<td>Designates that listing file will contain no page breaks</td>
</tr>
<tr>
<td><strong>PAGELENGTH ( N)</strong></td>
<td>P</td>
<td>PAGELENGTH(60)</td>
<td>PL</td>
<td>Sets maximum number of lines in each page of listing file (range=10 to 65536)</td>
</tr>
<tr>
<td><strong>PAGE WIDTH (N)</strong></td>
<td>P</td>
<td>PAGEWIDTH(120)</td>
<td>PW</td>
<td>Set maximum number of characters in each line of listing file (range = 72 to 132)</td>
</tr>
<tr>
<td><strong>PRINT( file)</strong></td>
<td>P</td>
<td>PRINT(source.LST)</td>
<td>PR</td>
<td>Designates file to receive source listing</td>
</tr>
<tr>
<td><strong>NOPRINT</strong></td>
<td>P</td>
<td>PRINT(source.LST)</td>
<td>NOPR</td>
<td>Designates that no listing file will be created</td>
</tr>
<tr>
<td><strong>SAVE</strong></td>
<td>G</td>
<td>not applicable</td>
<td>SA</td>
<td>Stores current control settings from SAVE stack</td>
</tr>
<tr>
<td><strong>RESTORE</strong></td>
<td>G</td>
<td>not applicable</td>
<td>RS</td>
<td>Restores control settings from SAVE stack</td>
</tr>
<tr>
<td><strong>REGISTERBANK (rb,...)</strong></td>
<td>P</td>
<td>REGISTERBANK(0)</td>
<td>RB</td>
<td>Indicates one or more banks used in program module</td>
</tr>
<tr>
<td><strong>NOREGISTERBANK</strong></td>
<td>P</td>
<td>REGISTERBANK(0)</td>
<td>NORB</td>
<td>Indicates that no register banks are used</td>
</tr>
<tr>
<td><strong>SYMBOLS</strong></td>
<td>P</td>
<td>SYMBOLS</td>
<td>SB</td>
<td>Creates a formatted table of all symbols used in program</td>
</tr>
<tr>
<td><strong>NOSYMBOLS</strong></td>
<td>P</td>
<td>SYMBOLS</td>
<td>NOSB</td>
<td>Designates that no symbol table is created</td>
</tr>
<tr>
<td><strong>TITLE( string)</strong></td>
<td>G</td>
<td>TITLE( )</td>
<td>TT</td>
<td>Places a string in all subsequent page headers (max. 60 characters)</td>
</tr>
<tr>
<td><strong>WORKFILES ( path)</strong></td>
<td>P</td>
<td>same as source</td>
<td>WF</td>
<td>Designates alternate path for temporary workfiles</td>
</tr>
<tr>
<td><strong>XREF</strong></td>
<td>P</td>
<td>NOXREF</td>
<td>XR</td>
<td>Creates a cross reference listing of all symbols used in program</td>
</tr>
<tr>
<td><strong>NOXREF</strong></td>
<td>P</td>
<td>NOXREF</td>
<td>NOXR</td>
<td>Designates that no cross reference list is created</td>
</tr>
</tbody>
</table>
MACROS

The macro processing facility (MPL) of ASM51 is a "string replacement" facility. Macros allow frequently used sections of code to be defined once using a simple mnemonic and used anywhere in the program by inserting the mnemonic. Programming using macros is a powerful extension of the techniques described thus far. Macros can be defined anywhere in a source program and subsequently used like any other instruction. The syntax for macro definition is

```
%*DEFINE (call_pattern) (macro_body)
```

Once defined, the call pattern is like a mnemonic; it may be used like any assembly language instruction by placing it in the mnemonic field of a program. Macros are made distinct from "real" instructions by preceding them with a percent sign, "%". When the source program is assembled, everything within the macro-body, on a character-by-character basis, is substituted for the call-pattern. The mystique of macros is largely unfounded. They provide a simple means for replacing cumbersome instruction patterns with primitive, easy-to-remember mnemonics. The substitution, we reiterate, is on a character-by-character basis—nothing more, nothing less.

For example, if the following macro definition appears at the beginning of a source file,

```
%*DEFINE (PUSH_DPTR)
  (PUSH DPH
  PUSH DPL)
```

then the statement

```
%PUSH_DPTR
```

will appear in the .LST file as

```
PUSH DPH
PUSH DPL
```

The example above is a typical macro. Since the 8051 stack instructions operate only on direct addresses, pushing the data pointer requires two PUSH instructions. A similar macro can be created to POP the data pointer.

There are several distinct advantages in using macros:

- A source program using macros is more readable, since the macro mnemonic is generally more indicative of the intended operation than the equivalent assembler instructions.
- The source program is shorter and requires less typing.
- Using macros reduces bugs
- Using macros frees the programmer from dealing with low-level details.

The last two points above are related. Once a macro is written and debugged, it is used freely without the worry of bugs. In the PUSH_DPTR example above, if PUSH and POP instructions are used rather than push and pop macros, the programmer may inadvertently reverse the order of the pushes or pops. (Was it the high-byte or low-byte that was pushed first?) This would create a bug. Using macros, however, the details are worked out once—when the macro is written—and the macro is used freely thereafter, without the worry of bugs.

Since the replacement is on a character-by-character basis, the macro definition should be carefully constructed with carriage returns, tabs, etc., to ensure proper alignment of the macro statements with the rest of the assembly language program. Some trial and error is required.

There are advanced features of ASM51's macro-processing facility that allow for parameter passing, local labels, repeat operations, assembly flow control, and so on. These are discussed below.
**Parameter Passing**

A macro with parameters passed from the main program has the following modified format:

\[
\%*\text{DEFINE} \quad \text{macro\_name\ (parameter\_list)} \quad \text{macro\_body}
\]

For example, if the following macro is defined,

\[
\%*\text{DEFINE} \quad \text{CMPA}\# \ (\text{VALUE})
\]

\[
\text{(CJNE} \quad \text{A, } \#\%\text{VALUE}, \$ + 3 \quad \text{)}
\]

then the macro call

\[
\%\text{CMPA}\# \ (20H)
\]

will expand to the following instruction in the .LST file:

\[
\text{CJNE} \quad \text{A, } \#20H, \$ + 3
\]

Although the 8051 does not have a "compare accumulator" instruction, one is easily created using the CJNE instruction with "$+3" (the next instruction) as the destination for the conditional jump. The CMPA# mnemonic may be easier to remember for many programmers. Besides, use of the macro unburdens the programmer from remembering notational details, such as "$+3."

Let's develop another example. It would be nice if the 8051 had instructions such as

- **JUMP IF ACCUMULATOR GREATER THAN X**
- **JUMP IF ACCUMULATOR GREATER THAN OR EQUAL TO X**
- **JUMP IF ACCUMULATOR LESS THAN X**
- **JUMP IF ACCUMULATOR LESS THAN OR EQUAL TO X**

but it does not. These operations can be created using CJNE followed by JC or JNC, but the details are tricky. Suppose, for example, it is desired to jump to the label GREATER_THAN if the accumulator contains an ASCII code greater than "Z" (5AH). The following instruction sequence would work:

\[
\text{CJNE} \quad \text{A, } \#5BH, \$ + 3 \\
\text{JNC GREATER_THAN}
\]

The CJNE instruction subtracts 5BH (i.e., "Z" + 1) from the content of A and sets or clears the carry flag accordingly. CJNE leaves C=1 for accumulator values 00H up to and including 5AH. (Note: 5AH-5BH<0, therefore C=1; but 5BH-5BH=0, therefore C=0.) Jumping to GREATER_THAN on the condition "not carry" correctly jumps for accumulator values 5BH, 5CH, 5DH, and so on, up to FFH. Once details such as these are worked out, they can be simplified by inventing an appropriate mnemonic, defining a macro, and using the macro instead of the corresponding instruction sequence. Here's the definition for a "jump if greater than" macro:

\[
\%*\text{DEFINE} \quad \text{JGT}(\text{VALUE, LABEL})
\]

\[
\text{(CJNE} \quad \text{A, } \#\%\text{VALUE+1, } \$ + 3 \quad ;\text{JGT} \\
\text{JNC } \quad \%\text{LABEL}
\)

To test if the accumulator contains an ASCII code greater than "Z," as just discussed, the macro would be called as

\[
\%\text{JGT} \quad ('Z', \text{GREATER_THAN})
\]

ASM51 would expand this into

\[
\text{CJNE} \quad \text{A, } \#5BH, \$ + 3 \quad ;\text{JGT} \\
\text{JNC GREATER_THAN}
\]

The JGT macro is an excellent example of a relevant and powerful use of macros. By using macros, the programmer benefits by using a meaningful mnemonic and avoiding messy and potentially bug-ridden details.
Local Labels

Local labels may be used within a macro using the following format:

```
%@DEFINE (macro_name [(parameter_list)])
[LOCAL list_of_local_labels] (macro_body)
```

For example, the following macro definition

```
%@DEFINE (DEC_DPTR) LOCAL SKIP
  (DEC DPL ;DECREMENT DATA POINTER
  MOV A, DPL
  CJNE A, #0FFH, %SKIP
  DEC DPL
%SKIP:
)
```

would be called as

```
%DEC_DPTR
```

and would be expanded by ASM51 into

```
DEC DPL ;DECREMENT DATA POINTER
MOV A, DPL
CJNE A, #0FFH, SKIP00
DEC DPH
SKIP00:
```

Note that a local label generally will not conflict with the same label used elsewhere in the source program, since ASM51 appends a numeric code to the local label when the macro is expanded. Furthermore, the next use of the same local label receives the next numeric code, and so on.

The macro above has a potential "side effect." The accumulator is used as a temporary holding place for DPL. If the macro is used within a section of code that uses A for another purpose, the value in A would be lost. This side effect probably represents a bug in the program. The macro definition could guard against this by saving A on the stack. Here's an alternate definition for the DEC_DPTR macro:

```
%@DEFINE (DEC_DPTR) LOCAL SKIP
  (PUSHACC
  DEC DPL ;DECREMENT DATA POINTER
  MOV A, DPL
  CJNE A, #0FFH, SKIP00
  DEC DPH
  SKIP00:
  POP ACC
)
```

Repeat Operations

This is one of several built-in (predefined) macros. The format is

```
%REPEAT (expression) (text)
```

For example, to fill a block of memory with 100 NOP instructions,

```
%REPEAT (100)
  (NOP)
```
Control Flow Operations

The conditional assembly of section of code is provided by ASM51's control flow macro definition. The format is

```
%IF (expression) THEN (balanced_text)
[ELSE (balanced_text)] FI
```

For example,

```
INTRENAL EQU 1 ; 1 = 8051 SERIAL I/O DRIVERS
 ; 0 = 8251 SERIAL I/O DRIVERS

%IF (INTERNAL) THEN
(INCHAR: ; 8051 DRIVERS

OUTCHR: ;

) ELSE
(INCHAR: ; 8251 DRIVERS

OUTCHR: ;

)
```

In this example, the symbol INTERNAL is given the value 1 to select I/O subroutines for the 8051's serial port, or the value 0 to select I/O subroutines for an external UART, in this case the 8251. The IF macro causes ASM51 to assemble one set of drivers and skip over the other. Elsewhere in the program, the INCHAR and OUTCHR subroutines are used without consideration for the particular hardware configuration. As long as the program as assembled with the correct value for INTERNAL, the correct subroutine is executed.
Appendix B: 8051 C Programming

ADVANTAGES AND DISADVANTAGES OF 8051 C

The advantages of programming the 8051 in C as compared to assembly are:

- Offers all the benefits of high-level, structured programming languages such as C, including the ease of writing subroutines
- Often relieves the programmer of the hardware details that the compiler handles on behalf of the programmer
- Easier to write, especially for large and complex programs
- Produces more readable program source codes

Nevertheless, 8051 C, being very similar to the conventional C language, also suffers from the following disadvantages:

- Processes the disadvantages of high-level, structured programming languages.
- Generally generates larger machine codes
- Programmer has less control and less ability to directly interact with hardware

To compare between 8051 C and assembly language, consider the solutions to the Example—Write a program using Timer 0 to create a 1KHz square wave on P1.0.

A solution written below in 8051 C language:

```c
sbit portbit = P1^0;  /*Use variable portbit to refer to P1.0*/
main ( )
{
    TMOD = 1;
    while (1)
    {
        TH0 = 0xFE;
        TL0 = 0xC;
        TR0 = 1;
        while (TF0 !=1);
        TR0 = 0;
        TF0 = 0;
        portbit = !(P1.^0);
    }
}
```

A solution written below in assembly language:

```assembly
ORG 8100H
MOV TMOD, #01H ;16-bit timer mode
LOOP:  MOV TH0, #0FEH ;500 (high byte)
        MOV TL0, #0CH ;500 (low byte)
        SETB TR0  ;start timer
        WAIT:  JNB TF0, WAIT ;wait for overflow
               CLR TR0  ;stop timer
               CLR TF0  ;clear timer overflow flag
               CPL P1.0 ;toggle port bit
               SJMP LOOP ;repeat
END
```

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Notice that both the assembly and C language solutions for the above example require almost the same number of lines. However, the difference lies in the readability of these programs. The C version seems more human than assembly, and is hence more readable. This often helps facilitate the human programmer's efforts to write even very complex programs. The assembly language version is more closely related to the machine code, and though less readable, often results in more compact machine code. As with this example, the resultant machine code from the assembly version takes 83 bytes while that of the C version requires 149 bytes, an increase of 79.5%!

The human programmer's choice of either high-level C language or assembly language for talking to the 8051, whose language is machine language, presents an interesting picture, as shown in following figure.

8051 C COMPILERS

We saw in the above figure that a compiler is needed to convert programs written in 8051 C language into machine language, just as an assembler is needed in the case of programs written in assembly language. A compiler basically acts just like an assembler, except that it is more complex since the difference between C and machine language is far greater than that between assembly and machine language. Hence the compiler faces a greater task to bridge that difference.

Currently, there exist various 8051 C compiler, which offer almost similar functions. All our examples and programs have been compiled and tested with Keil's μ Vision 2 IDE by Keil Software, an integrated 8051 program development environment that includes its C51 cross compiler for C. A cross compiler is a compiler that normally runs on a platform such as IBM compatible PCs but is meant to compile programs into codes to be run on other platforms such as the 8051.

DATA TYPES

8051 C is very much like the conventional C language, except that several extensions and adaptations have been made to make it suitable for the 8051 programming environment. The first concern for the 8051 C programmer is the data types. Recall that a data type is something we use to store data. Readers will be familiar with the basic C data types such as int, char, and float, which are used to create variables to store integers, characters, or floating-points. In 8051 C, all the basic C data types are supported, plus a few additional data types meant to be used specifically with the 8051.

The following table gives a list of the common data types used in 8051 C. The ones in bold are the specific 8051 extensions. The data type `bit` can be used to declare variables that reside in the 8051's bit-addressable locations (namely byte locations 20H to 2FH or bit locations 00H to 7FH). Obviously, these bit variables can only store bit values of either 0 or 1. As an example, the following C statement:

```c
bit flag = 0;
```

declares a bit variable called `flag` and initializes it to 0.
Data types used in 8051 C language

<table>
<thead>
<tr>
<th>Data Type</th>
<th>Bits</th>
<th>Bytes</th>
<th>Value Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit</td>
<td>1</td>
<td>0</td>
<td>0 to 1</td>
</tr>
<tr>
<td>signed char</td>
<td>8</td>
<td>1</td>
<td>-128 to +127</td>
</tr>
<tr>
<td>unsigned char</td>
<td>8</td>
<td>1</td>
<td>0 to 255</td>
</tr>
<tr>
<td>enum</td>
<td>16</td>
<td>2</td>
<td>-32768 to +32767</td>
</tr>
<tr>
<td>signed short</td>
<td>16</td>
<td>2</td>
<td>-32768 to +32767</td>
</tr>
<tr>
<td>unsigned short</td>
<td>16</td>
<td>2</td>
<td>0 to 65535</td>
</tr>
<tr>
<td>signed int</td>
<td>16</td>
<td>2</td>
<td>-32768 to +32767</td>
</tr>
<tr>
<td>unsigned int</td>
<td>16</td>
<td>2</td>
<td>0 to 65535</td>
</tr>
<tr>
<td>signed long</td>
<td>32</td>
<td>4</td>
<td>-2,147,483,648 to +2,147,483,647</td>
</tr>
<tr>
<td>unsigned long</td>
<td>32</td>
<td>4</td>
<td>0 to 4,294,967,295</td>
</tr>
<tr>
<td>float</td>
<td>32</td>
<td>4</td>
<td>±1.175494E-38 to ±3.402823E+38</td>
</tr>
<tr>
<td>sbit</td>
<td>1</td>
<td>0</td>
<td>0 to 1</td>
</tr>
<tr>
<td>sfr</td>
<td>8</td>
<td>1</td>
<td>0 to 255</td>
</tr>
<tr>
<td>sfr16</td>
<td>16</td>
<td>2</td>
<td>0 to 65535</td>
</tr>
</tbody>
</table>

The data type `sbit` is somewhat similar to the bit data type, except that it is normally used to declare 1-bit variables that reside in special function registes (SFRs). For example:

```c
sbit P = 0xD0;
```

declares the `sbit` variable `P` and specifies that it refers to bit address D0H, which is really the LSB of the PSW SFR. Notice the difference here in the usage of the assignment ("=") operator. In the context of `sbit` declarations, it indicatees what address the `sbit` variable resides in, while in `bit` declarations, it is used to specify the initial value of the `bit` variable.

Besides directly assigning a bit address to an `sbit` variable, we could also use a previously defined `sfr` variable as the base address and assign our `sbit` variable to refer to a certain bit within that `sfr`. For example:

```c
sfr PSW = 0xA8;
sbit P = PSW^0;
```

This declares an `sfr` variable called PSW that refers to the byte address D0H and then uses it as the base address to refer to its LSB (bit 0). This is then assigned to an `sbit` variable, `P`. For this purpose, the carat symbol (^) is used to specify bit position 0 of the PSW.

A third alternative uses a constant byte address as the base address within which a certain bit is referred. As an illustration, the previous two statements can be replaced with the following:

```c
sbit P = 0xD0 ^ 0;
```

Meanwhile, the `sfr` data type is used to declare byte (8-bit) variables that are associated with SFRs. The statement:

```c
sfr IE = 0xA8;
```

declares an `sfr` variable `IE` that resides at byte address A8H. Recall that this address is where the Interrupt Enable (IE) SFR is located; therefore, the `sfr` data type is just a means to enable us to assign names for SFRs so that it is easier to remember.

The `sfr16` data type is very similar to `sfr` but, while the `sfr` data type is used for 8-bit SFRs, `sfr16` is used for 16-bit SFRs. For example, the following statement:

```c
sfr16 DPTR = 0x82;
```
declares a 16-bit variable DPTR whose lower-byte address is at 82H. Checking through the 8051 architecture, we find that this is the address of the DPL SFR, so again, the `sfr16` data type makes it easier for us to refer to the SFRs by name rather than address. There's just one thing left to mention. When declaring `sbit`, `sfr`, or `sfr16` variables, remember to do so outside main, otherwise you will get an error.

In actual fact though, all the SFRs in the 8051, including the individual flag, status, and control bits in the bit-addressable SFRs have already been declared in an include file, called reg51.h, which comes packaged with most 8051 C compilers. By using reg51.h, we can refer for instance to the interrupt enable register as simply IE rather than having to specify the address A8H, and to the data pointer as DPTR rather than 82H. All this makes 8051 C programs more human-readable and manageable. The contents of reg51.h are listed below.

```c
/*--------------------------------------------------------------------------------------------------------------------
REG51.H
Header file for generic 8051 microcontroller.
----------------------------------------------------------------------------------------------------------------------*/

/* BYTE Register */

sfr    P0 = 0x80;
sfr    P1 = 0x90;
sfr    P2 = 0xA0;
sfr    P3 = 0xB0;
sfr    PSW = 0xD0;
sfr    ACC = 0xE0;
sfr    B = 0xF0;
sfr    SP = 0x81;
sfr    DPL = 0x82;
sfr    DPH = 0x83;
sfr    PCON = 0x87;
sfr    TCON = 0x88;
sfr    TMOD = 0x89;
sfr    TL0 = 0x8A;
sfr    TL1 = 0x8B;
sfr    TH0 = 0x8C;
sfr    TH1 = 0x8D;

/* SFR */

sbit    IE1 = 0xB8;
sbit    IT1 = 0x8A;
sbit    IE0 = 0x89;
sbit    IT0 = 0x88;
sbit    EA  = 0xAF;
sbit    ES = 0xAC;
sbit    ET1 = 0xAB;
sbit    EX1 = 0xAA;
sbit    ET0 = 0xA9;
sbit    EX0 = 0xA8;
sbit    PS = 0xBC;
sbit    PT1 = 0xBB;
sbit    PX1 = 0xBA;
sbit    PT0 = 0xB9;
sbit    PX0 = 0xB8;

/* PSW */

sbit    CY  = 0xD7;
sbit    AC = 0xD6;
sbit    F0 = 0xD5;

/* TCON */

sbit    TF1 = 0x8F;
sbit    TR1 = 0x8E;
sbit    TF0 = 0x8D;
sbit    TR0 = 0x8C;

/* SCON */

sbit    SM0 = 0x9F;
sbit    SM1 = 0x9E;
sbit    SM2 = 0x9D;
sbit    REN = 0x9C;

/* IE */

sbit    EA = 0xAF;
sbit    ES = 0xAC;
sbit    ET1 = 0xAB;
sbit    EX1 = 0xAA;
sbit    ET0 = 0xA9;
sbit    EX0 = 0xA8;

/* IP */

sbit    PS = 0xBC;
sbit    PT1 = 0xBB;
sbit    PX1 = 0xBA;
sbit    PT0 = 0xB9;
sbit    PX0 = 0xB8;

/* BIT */

sbit    RD = 0xB7;
sbit    WR = 0xB6;
sbit    T1 = 0xB5;
sbit    T0 = 0xB4;
sbit    INT1 = 0xB3;
sbit    INT0 = 0xB2;
sbit    TXD = 0xB1;
sbit    RXD = 0xB0;

/* SFR */

sbit    SM0 = 0x9F;
sbit    SM1 = 0x9E;
sbit    SM2 = 0x9D;
sbit    REN = 0x9C;

/* SCON */

sbit    SM0 = 0x9F;
sbit    SM1 = 0x9E;
sbit    SM2 = 0x9D;
sbit    REN = 0x9C;
```
MEMORY TYPES AND MODELS

The 8051 has various types of memory space, including internal and external code and data memory. When declaring variables, it is hence reasonable to wonder in which type of memory those variables would reside. For this purpose, several memory type specifiers are available for use, as shown in following table.

<table>
<thead>
<tr>
<th>Memory Types used in 8051 C language</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Type</td>
</tr>
<tr>
<td>code</td>
</tr>
<tr>
<td>data</td>
</tr>
<tr>
<td>idata</td>
</tr>
<tr>
<td>bdata</td>
</tr>
<tr>
<td>xdata</td>
</tr>
<tr>
<td>pdata</td>
</tr>
</tbody>
</table>

The first memory type specifier given in above table is `code`. This is used to specify that a variable is to reside in code memory, which has a range of up to 64 Kbytes. For example:

```c
char code errormsg[ ] = "An error occurred";
```

declares a char array called errormsg that resides in code memory.

If you want to put a variable into data memory, then use either of the remaining five data memory specifiers in above table. Though the choice rests on you, bear in mind that each type of data memory affect the speed of access and the size of available data memory. For instance, consider the following declarations:

```c
signed int   data num1;
bit  bdata numbit;
unsigned int xdata num2;
```

The first statement creates a signed int variable num1 that resides in internal data memory (00H to 7FH). The next line declares a bit variable numbit that is to reside in the bit-addressable memory locations (byte addresses 20H to 2FH), also known as `bdata`. Finally, the last line declares an unsigned int variable called num2 that resides in external data memory, `xdata`. Having a variable located in the directly addressable internal data memory speeds up access considerably; hence, for programs that are time-critical, the variables should be of type `data`. For other variants such as 8052 with internal data memory up to 256 bytes, the `idata` specifier may be used. Note however that this is slower than data since it must use indirect addressing. Meanwhile, if you would rather have your variables reside in external memory, you have the choice of declaring them as `pdata` or `xdata`. A variable declared to be in `pdata` resides in the first 256 bytes (a page) of external memory, while if more storage is required, `xdata` should be used, which allows for accessing up to 64 Kbytes of external data memory.

What if when declaring a variable you forget to explicitly specify what type of memory it should reside in, or you wish that all variables are assigned a default memory type without having to specify them one by one? In this case, we make use of `memory models`. The following table lists the various memory models that you can use.

<table>
<thead>
<tr>
<th>Memory models used in 8051 C language</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Model</td>
</tr>
<tr>
<td>Small</td>
</tr>
<tr>
<td>Compact</td>
</tr>
<tr>
<td>Large</td>
</tr>
</tbody>
</table>
A program is explicitly selected to be in a certain memory model by using the C directive, `#pragma`. Otherwise, the default memory model is **small**. It is recommended that programs use the small memory model as it allows for the fastest possible access by defaulting all variables to reside in internal data memory.

The **compact** memory model causes all variables to default to the first page of external data memory while the **large** memory model causes all variables to default to the full external data memory range of up to 64 Kbytes.

### ARRAYS

Often, a group of variables used to store data of the same type need to be grouped together for better readability. For example, the ASCII table for decimal digits would be as shown below.

<table>
<thead>
<tr>
<th>Decimal Digit</th>
<th>ASCII Code In Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>30H</td>
</tr>
<tr>
<td>1</td>
<td>31H</td>
</tr>
<tr>
<td>2</td>
<td>32H</td>
</tr>
<tr>
<td>3</td>
<td>33H</td>
</tr>
<tr>
<td>4</td>
<td>34H</td>
</tr>
<tr>
<td>5</td>
<td>35H</td>
</tr>
<tr>
<td>6</td>
<td>36H</td>
</tr>
<tr>
<td>7</td>
<td>37H</td>
</tr>
<tr>
<td>8</td>
<td>38H</td>
</tr>
<tr>
<td>9</td>
<td>39H</td>
</tr>
</tbody>
</table>

To store such a table in an 8051 C program, an array could be used. An array is a group of variables of the same data type, all of which could be accessed by using the name of the array along with an appropriate index.

The array to store the decimal ASCII table is:

```c
int table[10] = {0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39};
```

Notice that all the elements of an array are separated by commas. To access an individual element, an index starting from 0 is used. For instance, `table[0]` refers to the first element while `table[9]` refers to the last element in this ASCII table.

### STRUCTURES

Sometime it is also desired that variables of different data types but which are related to each other in some way be grouped together. For example, the name, age, and date of birth of a person would be stored in different types of variables, but all refer to the person's personal details. In such a case, a structure can be declared. A structure is a group of related variables that could be of different data types. Such a structure is declared by:

```c
struct
  person { char name;
           int age;
           long DOB;
  };
```

Once such a structure has been declared, it can be used like a data type specifier to create structure variables that have the member's name, age, and DOB. For example:

```c
struct
  person grace = {"Grace", 22, 01311980};
```
would create a structure variable grace to store the name, age, and data of birth of a person called Grace. Then in order to access the specific members within the person structure variable, use the variable name followed by the dot operator (.) and the member name. Therefore, grace.name, grace.age, grace.DOB would refer to Grace's name, age, and data of birth, respectively.

POINTERS

When programming the 8051 in assembly, sometimes register such as R0, R1, and DPTR are used to store the addresses of some data in a certain memory location. When data is accessed via these registers, indirect addressing is used. In this case, we say that R0, R1, or DPTR are used to point to the data, so they are essentially pointers.

Correspondingly in C, indirect access of data can be done through specially defined pointer variables. Pointers are simply just special types of variables, but whereas normal variables are used to directly store data, pointer variables are used to store the addresses of the data. Just bear in mind that whether you use normal variables or pointer variables, you still get to access the data in the end. It is just whether you go directly to where it is stored and get the data, as in the case of normal variables, or first consult a directory to check the location of that data before going there to get it, as in the case of pointer variables.

Declaring a pointer follows the format:

```
data_type    *pointer_name;
```

where

- `data_type` refers to which type of data that the pointer is pointing to
- `*` denotes that this is a pointer variable
- `pointer_name` is the name of the pointer

As an example, the following declarations:

```c
int    * numPtr
int    num;
numPtr = &num;
```

first declares a pointer variable called numPtr that will be used to point to data of type int. The second declaration declares a normal variable and is put there for comparison. The third line assigns the address of the num variable to the numPtr pointer. The address of any variable can be obtained by using the address operator, &, as is used in this example. Bear in mind that once assigned, the numPtr pointer contains the address of the num variable, not the value of its data.

The above example could also be rewritten such that the pointer is straightaway initialized with an address when it is first declared:

```c
int    num;
int    * numPtr = &num;
```

In order to further illustrate the difference between normal variables and pointer variables, consider the following, which is not a full C program but simply a fragment to illustrate our point:

```c
int    num = 7;
int    * numPtr = &num;
printf("%d\n", num);
printf("%d\n", numPtr);
printf("%d\n", &num);
printf("%d\n", *numPtr);
```
The first line declare a normal variable, num, which is initialized to contain the data 7. Next, a pointer variable, numPtr, is declared, which is initialized to point to the address of num. The next four lines use the printf( ) function, which causes some data to be printed to some display terminal connected to the serial port. The first such line displays the contents of the num variable, which is in this case the value 7. The next displays the contents of the numPtr pointer, which is really some weird-looking number that is the address of the num variable. The third such line also displays the address of the num variable because the address operator is used to obtain num's address. The last line displays the actual data to which the numPtr pointer is pointing, which is 7. The * symbol is called the indirection operator, and when used with a pointer, indirectly obtains the data whose address is pointed to by the pointer. Therefore, the output display on the terminal would show:

7
13452  (or some other weird-looking number)
13452  (or some other weird-looking number)
7

A Pointer's Memory Type

Recall that pointers are also variables, so the question arises where they should be stored. When declaring pointers, we can specify different types of memory areas that these pointers should be in, for example:

```c
int    * xdata numPtr = & num;
```

This is the same as our previous pointer examples. We declare a pointer numPtr, which points to data of type int stored in the num variable. The difference here is the use of the memory type specifier `xdata` after the * . This is specifies that pointer numPtr should reside in external data memory (`xdata`), and we say that the pointer's memory type is `xdata`.

Typed Pointers

We can go even further when declaring pointers. Consider the example:

```c
int    data * xdata numPtr = & num;
```

The above statement declares the same pointer numPtr to reside in external data memory (`xdata`), and this pointer points to data of type int that is itself stored in the variable num in internal data memory (`data`). The memory type specifier, `data`, before the * specifies the `data memory type` while the memory type specifier, `xdata`, after the * specifies the pointer memory type.

Pointer declarations where the data memory types are explicitly specified are called typed pointers. Typed pointers have the property that you specify in your code where the data pointed by pointers should reside. The size of typed pointers depends on the data memory type and could be one or two bytes.

Untyped Pointers

When we do not explicitly state the data memory type when declaring pointers, we get untyped pointers, which are generic pointers that can point to data residing in any type of memory. Untyped pointers have the advantage that they can be used to point to any data independent of the type of memory in which the data is stored. All untyped pointers consist of 3 bytes, and are hence larger than typed pointers. Untyped pointers are also generally slower because the data memory type is not determined or known until the compiled program is run at runtime. The first byte of untyped pointers refers to the data memory type, which is simply a number according to the following table. The second and third bytes are, respectively, the higher-order and lower-order bytes of the address being pointed to.

An untyped pointer is declared just like normal C, where:

```c
int    * xdata numPtr = & num;
```

does not explicitly specify the memory type of the data pointed to by the pointer. In this case, we are using untyped pointers.
<table>
<thead>
<tr>
<th>Value</th>
<th>Data Memory Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>idata</td>
</tr>
<tr>
<td>2</td>
<td>xdata</td>
</tr>
<tr>
<td>3</td>
<td>pdata</td>
</tr>
<tr>
<td>4</td>
<td>data/bdata</td>
</tr>
<tr>
<td>5</td>
<td>code</td>
</tr>
</tbody>
</table>

**FUNCTIONS**

In programming the 8051 in assembly, we learnt the advantages of using subroutines to group together common and frequently used instructions. The same concept appears in 8051 C, but instead of calling them subroutines, we call them **functions**. As in conventional C, a function must be declared and defined. A function definition includes a list of the number and types of inputs, and the type of the output (return type), plus a description of the internal contents, or what is to be done within that function.

The format of a typical function definition is as follows:

```
return_type    function_name (arguments)    [memory]  [reentrant]  [interrupt]  [using]
{
    ...
}
```

where

- `return_type` refers to the data type of the return (output) value
- `function_name` is any name that you wish to call the function as
- `arguments` is the list of the type and number of input (argument) values
- `memory` refers to an explicit memory model (small, compact or large)
- `reentrant` refers to whether the function is reentrant (recursive)
- `interrupt` indicates that the function is actually an ISR
- `using` explicitly specifies which register bank to use

Consider a typical example, a function to calculate the sum of two numbers:

```
int  sum (int a, int b)
{
    return  a + b;
}
```

This function is called `sum` and takes in two arguments, both of type `int`. The return type is also int, meaning that the output (return value) would be an int. Within the body of the function, delimited by braces, we see that the return value is basically the sum of the two arguments. In our example above, we omitted explicitly specifying the options: memory, reentrant, interrupt, and using. This means that the arguments passed to the function would be using the default small memory model, meaning that they would be stored in internal data memory. This function is also by default non-recursive and a normal function, not an ISR. Meanwhile, the default register bank is bank 0.

**Parameter Passing**

In 8051 C, parameters are passed to and from functions and used as function arguments (inputs). Nevertheless, the technical details of where and how these parameters are stored are transparent to the programmer, who does not need to worry about these technicalities. In 8051 C, parameters are passed through the register or through memory. Passing parameters through registers is faster and is the default way in which things are done. The registers used and their purpose are described in more detail below.
Registers used in parameter passing

<table>
<thead>
<tr>
<th>Number of Argument</th>
<th>Char / 1-Byte Pointer</th>
<th>INT / 2-Byte Pointer</th>
<th>Long/Float</th>
<th>Generic Pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R7</td>
<td>R6 &amp; R7</td>
<td>R4–R7</td>
<td>R1–R3</td>
</tr>
<tr>
<td>2</td>
<td>R5</td>
<td>R4 &amp; R5</td>
<td>R4–R7</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>R2 &amp; R3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Since there are only eight registers in the 8051, there may be situations where we do not have enough registers for parameter passing. When this happens, the remaining parameters can be passed through fixed memory locations. To specify that all parameters will be passed via memory, the NOREGPARMs control directive is used. To specify the reverse, use the REGPARMS control directive.

Return Values

Unlike parameters, which can be passed by using either registers or memory locations, output values must be returned from functions via registers. The following table shows the registers used in returning different types of values from functions.

<table>
<thead>
<tr>
<th>Return Type</th>
<th>Register</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit</td>
<td>Carry Flag (C)</td>
<td></td>
</tr>
<tr>
<td>char/unsigned char/1-byte pointer</td>
<td>R7</td>
<td></td>
</tr>
<tr>
<td>int/unsigned int/2-byte pointer</td>
<td>R6 &amp; R7</td>
<td>MSB in R6, LSB in R7</td>
</tr>
<tr>
<td>long/unsigned long</td>
<td>R4–R7</td>
<td>MSB in R4, LSB in R7</td>
</tr>
<tr>
<td>float</td>
<td>R4–R7</td>
<td>32-bit IEEE format</td>
</tr>
<tr>
<td>generic pointer</td>
<td>R1–R3</td>
<td>Memory type in R3, MSB in R2, LSB in R1</td>
</tr>
</tbody>
</table>
### Appendix C: STC12C5A60S2 series MCU Electrical Characteristics

#### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage temperature</td>
<td>TST</td>
<td>-55</td>
<td>+125</td>
<td>℃</td>
</tr>
<tr>
<td>Operating temperature (I)</td>
<td>TA</td>
<td>-40</td>
<td>+85</td>
<td>℃</td>
</tr>
<tr>
<td>Operating temperature (C)</td>
<td>TA</td>
<td>0</td>
<td>+70</td>
<td>℃</td>
</tr>
<tr>
<td>DC power supply (5V)</td>
<td>VDD - VSS</td>
<td>-0.3</td>
<td>+5.5</td>
<td>V</td>
</tr>
<tr>
<td>DC power supply (3V)</td>
<td>VDD - VSS</td>
<td>-0.3</td>
<td>+3.6</td>
<td>V</td>
</tr>
<tr>
<td>Voltage on any pin</td>
<td>-</td>
<td>-0.3</td>
<td>VCC + 0.3</td>
<td>V</td>
</tr>
</tbody>
</table>

#### DC Specification (5V MCU)

<table>
<thead>
<tr>
<th>Sym</th>
<th>Parameter</th>
<th>Specification</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Operating Voltage</td>
<td>3.3</td>
<td>5.0</td>
</tr>
<tr>
<td>IPD</td>
<td>Power Down Current</td>
<td>-</td>
<td>&lt; 0.1</td>
</tr>
<tr>
<td>IIDL</td>
<td>Idle Current</td>
<td>-</td>
<td>3.0</td>
</tr>
<tr>
<td>ICC</td>
<td>Operating Current</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>VIL1</td>
<td>Input Low (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VIH1</td>
<td>Input High (P0,P1,P2,P3)</td>
<td>2.0</td>
<td>-</td>
</tr>
<tr>
<td>VIH2</td>
<td>Input High (RESET)</td>
<td>2.2</td>
<td>-</td>
</tr>
<tr>
<td>IOL1</td>
<td>Sink Current for output low (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IOH1</td>
<td>Sourcing Current for output high (P0,P1,P2,P3)</td>
<td>150</td>
<td>230</td>
</tr>
<tr>
<td>IOH2</td>
<td>Sourcing Current for output high (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IIL</td>
<td>Logic 0 input current (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>ITL</td>
<td>Logic 1 to 0 transition current (P0,P1,P2,P3)</td>
<td>100</td>
<td>270</td>
</tr>
</tbody>
</table>

#### DC Specification (3V MCU)

<table>
<thead>
<tr>
<th>Sym</th>
<th>Parameter</th>
<th>Specification</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Operating Voltage</td>
<td>2.2</td>
<td>3.3</td>
</tr>
<tr>
<td>IPD</td>
<td>Power Down Current</td>
<td>-</td>
<td>&lt;0.1</td>
</tr>
<tr>
<td>IIDL</td>
<td>Idle Current</td>
<td>-</td>
<td>2.0</td>
</tr>
<tr>
<td>ICC</td>
<td>Operating Current</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>VIL1</td>
<td>Input Low (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>VIH1</td>
<td>Input High (P0,P1,P2,P3)</td>
<td>2.0</td>
<td>-</td>
</tr>
<tr>
<td>VIH2</td>
<td>Input High (RESET)</td>
<td>2.2</td>
<td>-</td>
</tr>
<tr>
<td>IOL1</td>
<td>Sink Current for output low (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IOH1</td>
<td>Sourcing Current for output high (P0,P1,P2,P3)</td>
<td>40</td>
<td>70</td>
</tr>
<tr>
<td>IOH2</td>
<td>Sourcing Current for output high (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IIL</td>
<td>Logic 0 input current (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>ITL</td>
<td>Logic 1 to 0 transition current (P0,P1,P2,P3)</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Appendix D: Using Serial port expand I/O interface

STC12C5A60S2 series MCU serial port mode0 can be used for expand IO if UART is free in your application. UART Mode0 is a synchronous shift register, the baudrate is fixed at fosc/12, RXD pin (P3.0) is the data I/O port, and TXD pin (P3.1) is clock output port, data width is 8 bits, always sent / received the lowest bit at first.

(1) Using 74HC165 expand parallel input ports

Please refer to the following circuit which using 2 pcs 74HC165 to expand 16 input I/Os

74HC165 is a 8-bit parallel input shift register, when S/L (Shift/Load) pin is falling to low level, the parallel port data is read into internal register, and now, if S/L is raising to high and ClockDisable pin (15 pin) is low level, then clock signal from CP pin is enable. At this time register data will be output from the Dh pin (9 pin) with the clock input.

```
MOV R7,#05H ;read 5 groups data
MOV R0,#20H ;set buffer address
START: CLR P1.0 ;S/L = 0, load port data
    SETB P1.0 ;S/L = 1, lock data and enable clock
    MOV R1,#02H ;2 bytes per group
    RXDAT:MOV SCON,#00010000B       ;set serial as mode 0 and enable receive data
    WAIT: JNB RI,WAIT ;wait for receive complete
        CLR RI ;clear receive complete flag
        MOV A,SBUF ;read data to ACC
        MOV @R0,A ;save data to buffer
        INC R0 ;modify buffer ptr
        DJNZ R1,RXDAT ;read next byte
        DJNZ R7,START ;read next group
        ...
```

(2) Using 74HC164 expand parallel output ports

Please refer to the following circuit which using 2 pcs 74HC164 to expand 16 output I/Os

When serial port is working in MODE0, the serial data is input/output from RXD(P3.0) pin and serial clock is output from TXD(P3.1). Serial data is always starting transmission from the lowest bit.

START: MOV R7,#02H ;output 2 bytes data
       MOV R0,#30H ;set buffer address
       MOV SCON,#00000000B ;set serial as mode 0
SEND:  MOV A,@R0 ;read data from buffer
       MOV SBUF,A ;start send data
WAIT:   JNB TI,WAIT ;wait for send complete
       CLR TI ;clear send complete flag
       INC R0 ;modify buffer ptr
       DJNZ R7,SEND ;send next data
       ...
Appendix E: STC12C5Axx series MCU to replace traditional 8051 Notes

STC12C5Axx series MCU Timer0/Timer1/UART is fully compatible with the traditional 8051 MCU. After power on reset, the default input clock source is the divider 12 of system clock frequency, and UART baudrate generator is Timer 1. Add an independent Baud Rate Generator, saved the Timer2 in 8052 system. MCU instruction execution speed is faster than the traditional 8051 MCU 8 ~ 12 times in the same working environment, so software delay programs need to be adjusted.

ALE
Traditional 8051's ALE pin output signal on divide 6 the system clock frequency can be externally provided clock, if disable ALE output in STC12C5Axx series system, you can get clock source from CLKOUT0/P3.4, CLKOUT1/P3.5, CLKOUT2/P1.0 or XTAL2 clock output. (Recommended a 200ohm series resistor to the XTAL2 pin).

ALE pin is an disturbance source when traditional 8051's system clock frequency is too high. STC89xx series MCU add ALEOFFF bit in AUXR register. While STC12C5Axx series MCU directly disable ALE pin dividing 6 the system clock output, and can remove ALE disturbance thoroughly. Please compare the following two registers.

AUXR register of STC89xx series

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Add</th>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Reset Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUXR</td>
<td>8EH</td>
<td>Auxiliary register</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>EXTRAM</td>
<td>ALEOFF</td>
<td>xxx,xx00</td>
</tr>
</tbody>
</table>

AUXR register of STC12C5A60S2 series

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Add</th>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Reset Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUXR</td>
<td>8EH</td>
<td>Auxiliary register</td>
<td>T0x12</td>
<td>T1x12</td>
<td>UART_M0x6</td>
<td>BRTR</td>
<td>S2SMOD2</td>
<td>BRTx12</td>
<td>EXTRAM</td>
<td>S1BRS</td>
<td>0000,0000</td>
</tr>
</tbody>
</table>

PSEN
Traditional 8051 execute external program through the PSEN signal, STC12C5A60S2 series is system MCU concept, integrated high-capacity internal program memory, do not need external program memory expansion generally, so have no PSEN signal, PSEN pin can be used as GPIO.

General Quasi-Bidirectional I/O
Traditional 8051 access I/O (signal transition or read status) timing is 12 clocks, STC12C5A60S2 series MCU is 4 clocks. When you need to read an external signal, if internal output a rising edge signal, for the traditional 8051, this process is 12 clocks, you can read at once, but for STC12C5A60S2 series MCU, this process is 4 clocks, when internal instructions is complete but external signal is not ready, so you must delay 1~2 nop operation.

P4 port
STC12C5A60S2 series MCU has integral P4 port (P4.0~P4.7), and location at address C0H. No extended external interrupt INT2/INT3. STC12C5A60S2 series is difference from STC89 series (STC89 series MCU has half byte P4 port (P4.0~P4.3), location at address E8H, extended external interrupt INT2/INT3).

Port drive capability
STC12C5A60S2 series I/O port sink drive current is 20mA, has a strong drive capability, the port is not burn out when drive high current generally. STC89 series I/O port sink drive current is only 6mA, is not enough to drive high current. For the high current drive applications, it is strongly recommended to use STC12C5A60S2 series MCU.
WatchDog

STC12C5A60S2 series MCU’s watch dog timer control register (WDT_CONTR) is location at C1H, add watch dog reset flag.

STC12C5A60S2 series WDT_CONTR (C1H)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Add</th>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Reset Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDT_CONTR</td>
<td>C1H</td>
<td>Wact-Dog-Timer Control register</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx00,0000</td>
</tr>
<tr>
<td>WDT_FLAG</td>
<td></td>
<td></td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

STC89 series WDT_CONTR (E1H)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Add</th>
<th>Name</th>
<th>Bit7</th>
<th>Bit6</th>
<th>Bit5</th>
<th>Bit4</th>
<th>Bit3</th>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Reset Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDT_CONTR</td>
<td>E1H</td>
<td>Wact-Dog-Timer Control register</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>xx00,0000</td>
</tr>
</tbody>
</table>

STC12C5A60S2 series MCU auto enable watch dog timer after ISP upgrade, but not in STC89 series, so STC12C5A60S2 series’s watch dog is more reliable.

EEPROM

SFR associated with EEPROM

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>STC12Cxx Address</th>
<th>STC89xx Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IAP_DATA</td>
<td>C2H</td>
<td>E2H</td>
<td>ISP/IAP Flash data register</td>
</tr>
<tr>
<td>IAP_ADDRH</td>
<td>C3H</td>
<td>E3G</td>
<td>ISP/IAP Flash HIGH address register</td>
</tr>
<tr>
<td>IAP_ADDRL</td>
<td>C4H</td>
<td>E4H</td>
<td>ISP/IAP Flash LOW address register</td>
</tr>
<tr>
<td>IAP_CMD</td>
<td>C5H</td>
<td>E5H</td>
<td>ISP/IAP Flash command register</td>
</tr>
<tr>
<td>IAP_TRIG</td>
<td>C6H</td>
<td>E6H</td>
<td>ISP/IAP command trigger register</td>
</tr>
<tr>
<td>IAP_CONTR</td>
<td>C7H</td>
<td>E7H</td>
<td>ISP/IAP control register</td>
</tr>
</tbody>
</table>

STC12C5A60S2 series write 5AH and A5H sequential to trigger EEPROM flash command, and STC89 series write 46H and B9H sequential to trigger EEPROM flash command.

STC12C5A60S2 series EEPROM start address all location at 0000H, but STC89 series is not.

Internal/external clock source

STC12C5A60S2 series MCU has a optional internal RC oscillator. Generally, for 40/44 pin package MCU, set to use external crystal oscillator and for 20/18/16 pin package set to use internl RC oscillator in factory. When use ISP download program, user can arbitrarily choose internal RC oscillator or external crystal oscillator. STC89 series MCU can only choose external crystal oscillator.

Power consumption

Power consumption consists of two parts: crystal oscillator amplifier circuits and digital circuits. For crystal oscillator amplifier circuits, STC12C5A60S2 series is lower then STC89 series. For digital circuits, the higher clock frequency, the greater the power consumption. STC12C5A60S2 series MCU instruction execution speed is faster than the STC89 series MCU 3–24 times in the same working environment, so if you need to achieve the same efficiency, STC12C5A60S2 series required frequency is lower than STC89 series MCU.

PowerDown Wakeup

STC12C5Axx series MCU wake-up support for low level or falling edge depend on the external interrupt mode, but STC89 series only support for low level. In addition, STC12C5Axx series have a Optional power-down wake-up delay length : 32768 / 16384 / 8192 / 4096 clocks.
About reset circuit
If the system frequency is below 12MHz, the external reset circuit is not required. Reset pin can be connected
to ground through the 1K resistor or can be connected directly to ground. The proposal to create PCB to
retain RC reset circuit

About Clock oscillator
If you need to use internal RC oscillator, XTAL1 pin and XTAL2 pin must be floating. If you use a external
active crystal oscillator, clock signal input from XTAL1 pin and XTAL2 pin floating.

About power
Power at both ends need to add a 47uF electrolytic capacitor and a 0.1uF capacitor, to remove the coupling
and filtering.
## Appendix F: STC12C5A60S2 series Selection Table

<table>
<thead>
<tr>
<th>Type 1T 8051 MCU</th>
<th>Operating voltage (V)</th>
<th>Flash (B)</th>
<th>S RAM (B)</th>
<th>TIMER</th>
<th>UART</th>
<th>DPORT</th>
<th>16-bit PCA/8-bit PWM D/A</th>
<th>A/D</th>
<th>WDT</th>
<th>EEPROM (B)</th>
<th>External reset threshold voltage can be configured</th>
<th>External interrupts which can wake up power down mode</th>
<th>Special timer for waking power down mode</th>
<th>Package of 40-pin (36 I/O ports)</th>
<th>Package of 44-pin (40 I/O ports)</th>
<th>Package of 48-pin (44 I/O ports)</th>
</tr>
</thead>
<tbody>
<tr>
<td>STC12C5A08S2</td>
<td>5.5~3.5</td>
<td>8K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>53K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A16S2</td>
<td>5.5~3.5</td>
<td>16K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>45K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A32S2</td>
<td>5.5~3.5</td>
<td>32K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>29K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A40S2</td>
<td>5.5~3.5</td>
<td>40K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>21K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A48S2</td>
<td>5.5~3.5</td>
<td>48K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>13K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A52S2</td>
<td>5.5~3.5</td>
<td>52K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>9K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A56S2</td>
<td>5.5~3.5</td>
<td>56K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>5K</td>
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<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12C5A60S2</td>
<td>5.5~3.5</td>
<td>60K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>1K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>IAP12C5A62S2</td>
<td>5.5~3.5</td>
<td>62K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>IAP</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>Type 1T 8051 MCU</td>
<td>Operating voltage (V)</td>
<td>Flash (B)</td>
<td>S RAM (B)</td>
<td>TIMER</td>
<td>UART</td>
<td>DPORT</td>
<td>16-bit PCA/8-bit PWM D/A</td>
<td>A/D</td>
<td>WDT</td>
<td>EEPROM (B)</td>
<td>External reset threshold voltage can be configured</td>
<td>External interrupts which can wake up power down mode</td>
<td>Special timer for waking power down mode</td>
<td>Package of 40-pin (36 I/O ports)</td>
<td>Package of 44-pin (40 I/O ports)</td>
<td>Package of 48-pin (44 I/O ports)</td>
</tr>
<tr>
<td>STC12LE5A08S2</td>
<td>3.6~2.1</td>
<td>8K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
<td>53K</td>
<td>Y</td>
<td>Y</td>
<td>7</td>
<td>N</td>
<td>PDIP</td>
<td>LQFP/PLCC</td>
</tr>
<tr>
<td>STC12LE5A16S2</td>
<td>3.6~2.1</td>
<td>16K</td>
<td>1280</td>
<td>4</td>
<td>2-3</td>
<td>2</td>
<td>2</td>
<td>10</td>
<td>Y</td>
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<td>Timer</td>
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<td>Special timer for waking power down mode</td>
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<td>Package of 44-pin (40 I/O ports)</td>
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**Notes:**
- The above table details various types of 1T 8051 MCUs with different specifications.
- The table entries include key features such as operating voltage, flash memory, SRAM, timer, UART, D/A, WDT, EEPROM, external real-time low voltage interrupt, external reset threshold voltage configuration, and package types.
- Specific models include STC12C5A08AD, STC12C5A16AD, STC12C5A32AD, STC12C5A40AD, STC12C5A48AD, STC12C5A52AD, STC12C5A56AD, STC12C5A60AD, IAP12C5A62AD, STC12LE5A08AD, STC12LE5A16AD, STC12LE5A32AD, STC12LE5A40AD, STC12LE5A48AD, STC12LE5A52AD, STC12LE5A56AD, STC12LE5A60AD, IAP12LE5A62AD.
- The table provides a comprehensive overview of the various 1T 8051 MCUs available, highlighting their unique capabilities and specifications.

**Contact:**
- Website: www.STCMCU.com
- Mobile: (86)13922805190
- Tel: 86-755-82948412
- Fax: 86-755-82944243
| Type IT 8051 MCU | Operating voltage (V) | Flash (B) | SRAM (B) | TIMER | UART | 16-bit PCA/8-bit PWM D/A | A/D | WDT | EEPROM (B) | External real-time low voltage interrupt | External Reset threshold voltage can be configured | External interrupts which can wake up power down mode | Special timer for waking power down mode | Package of 40-pin (36 I/O ports) | Package of 44-pin (40 I/O ports) | Package of 48-pin (44 I/O ports) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| STC12C5A08PWM | 5.5~3.5 | 8K | 1280 | 4 | 1 | 2 | 2 | N | Y | 53K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A16PWM | 5.5~3.5 | 16K | 1280 | 4 | 1 | 2 | 2 | N | Y | 45K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A32PWM | 5.5~3.5 | 32K | 1280 | 4 | 1 | 2 | 2 | N | Y | 29K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A40PWM | 5.5~3.5 | 40K | 1280 | 4 | 1 | 2 | 2 | N | Y | 21K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A48PWM | 5.5~3.5 | 48K | 1280 | 4 | 1 | 2 | 2 | N | Y | 13K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A52PWM | 5.5~3.5 | 52K | 1280 | 4 | 1 | 2 | 2 | N | Y | 9K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A56PWM | 5.5~3.5 | 56K | 1280 | 4 | 1 | 2 | 2 | N | Y | 5K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12C5A60PWM | 5.5~3.5 | 60K | 1280 | 4 | 1 | 2 | 2 | N | Y | 1K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| IAP12C5A62PWM | 5.5~3.5 | 62K | 1280 | 4 | 1 | 2 | 2 | N | Y | IAP | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| Type IT 8051 MCU | Operating voltage (V) | Flash (B) | SRAM (B) | TIMER | UART | 16-bit PCA/8-bit PWM D/A | A/D | WDT | EEPROM (B) | External real-time low voltage interrupt | External Reset threshold voltage can be configured | External interrupts which can wake up power down mode | Special timer for waking power down mode | Package of 40-pin (36 I/O ports) | Package of 44-pin (40 I/O ports) | Package of 48-pin (44 I/O ports) |
| STC12LE5A08PWM | 3.6~2.1 | 8K | 1280 | 4 | 1 | 2 | 2 | N | Y | 53K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A16PWM | 3.6~2.1 | 16K | 1280 | 4 | 1 | 2 | 2 | N | Y | 45K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A32PWM | 3.6~2.1 | 32K | 1280 | 4 | 1 | 2 | 2 | N | Y | 29K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A40PWM | 3.6~2.1 | 40K | 1280 | 4 | 1 | 2 | 2 | N | Y | 21K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A48PWM | 3.6~2.1 | 48K | 1280 | 4 | 1 | 2 | 2 | N | Y | 13K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A52PWM | 3.6~2.1 | 52K | 1280 | 4 | 1 | 2 | 2 | N | Y | 9K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A56PWM | 3.6~2.1 | 56K | 1280 | 4 | 1 | 2 | 2 | N | Y | 5K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| STC12LE5A60PWM | 3.6~2.1 | 60K | 1280 | 4 | 1 | 2 | 2 | N | Y | 1K | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |
| IAP12LE5A62PWM | 3.6~2.1 | 62K | 1280 | 4 | 1 | 2 | 2 | N | Y | IAP | Y | 7 | N | PDIP | LQFP/PLCC | LQFP-48 |